

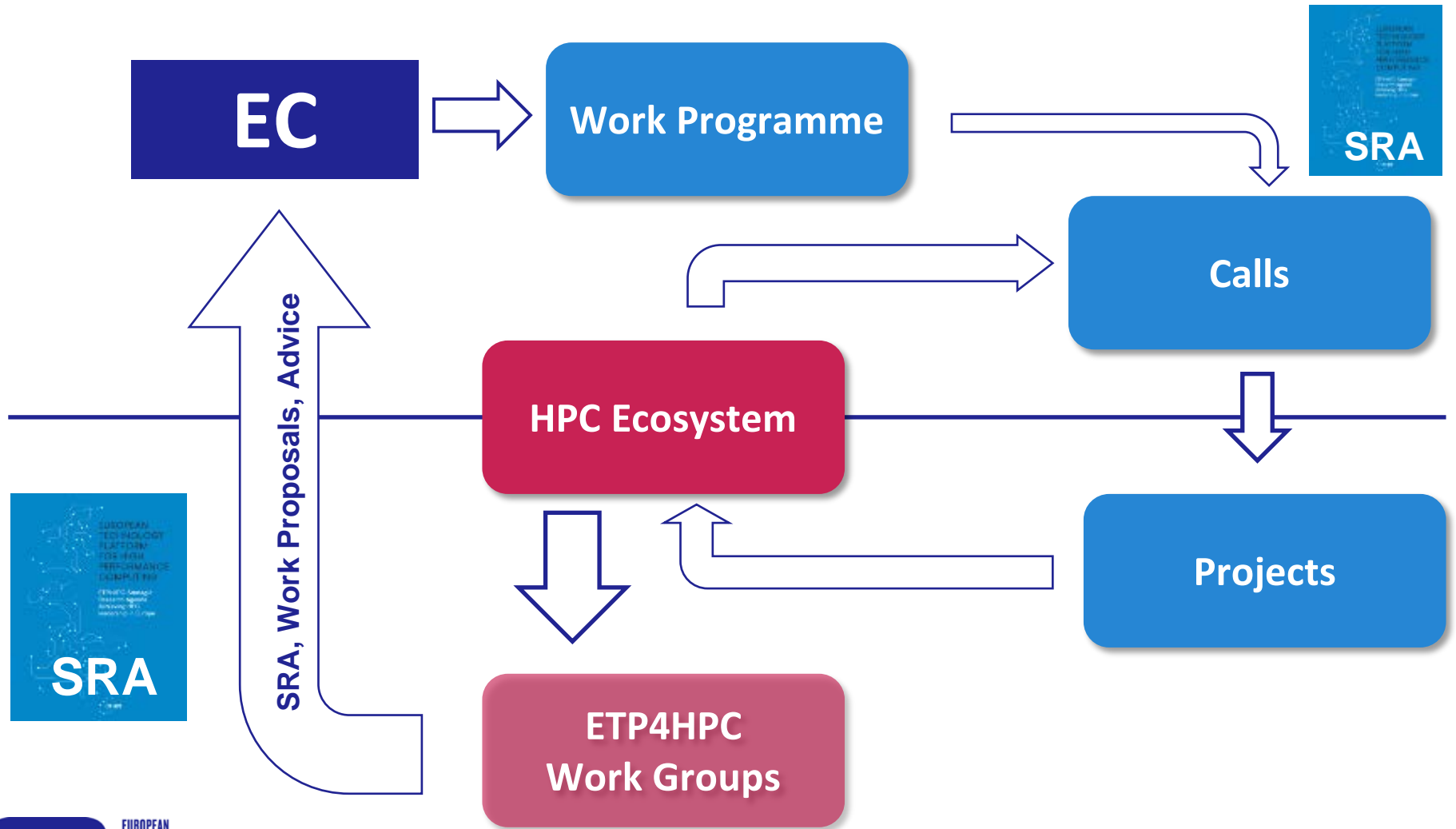


WORKPROGRAMME 2018-2020 RECOMMENDATIONS

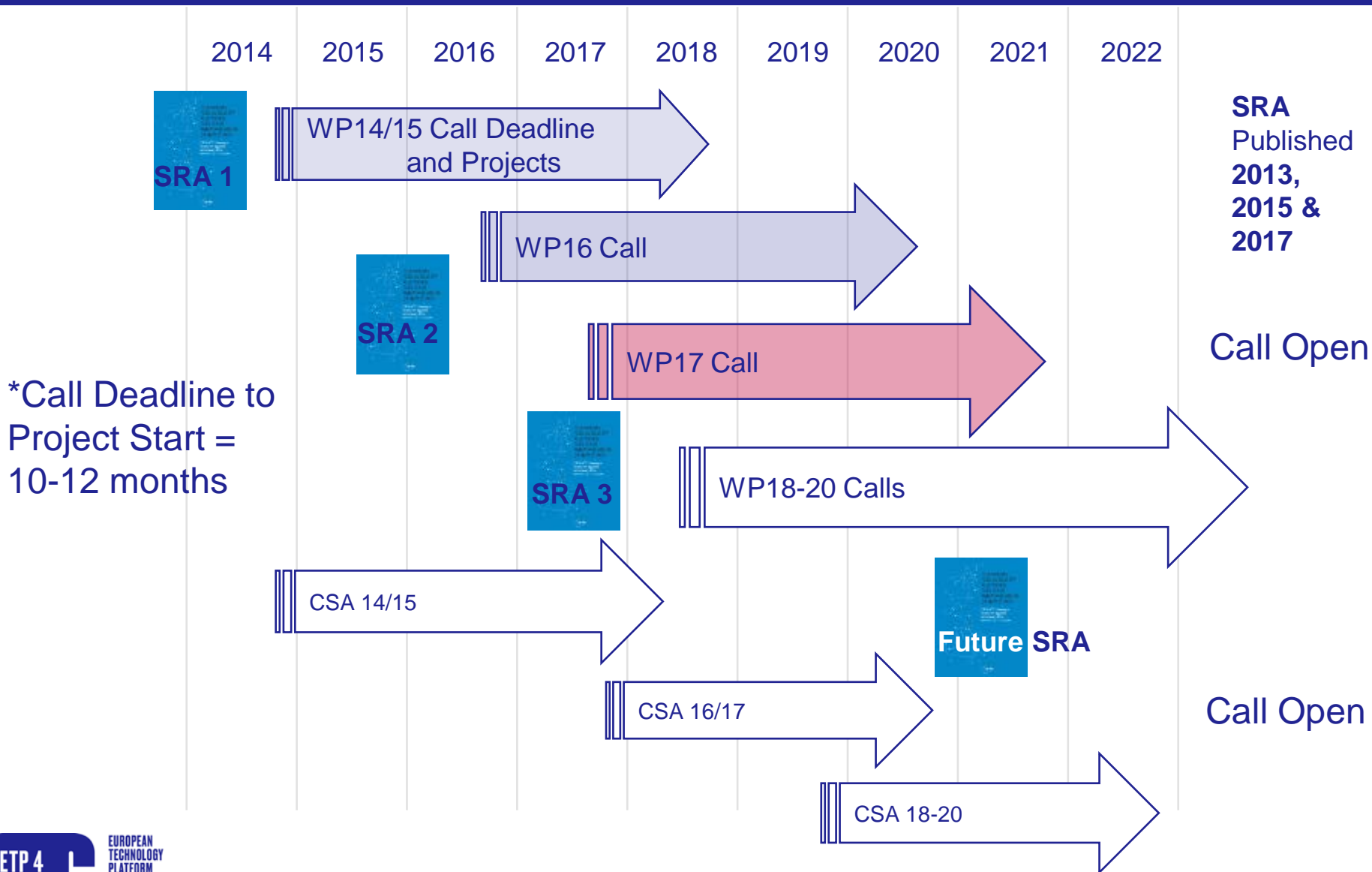
Our Multi-Annual HPC Technology Roadmap

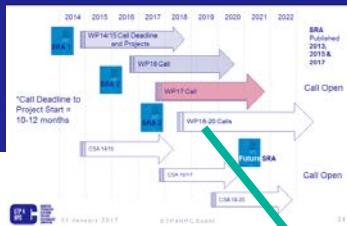
www.etp4hpc.eu/sra

SRAs AND WPs: THE FLOW

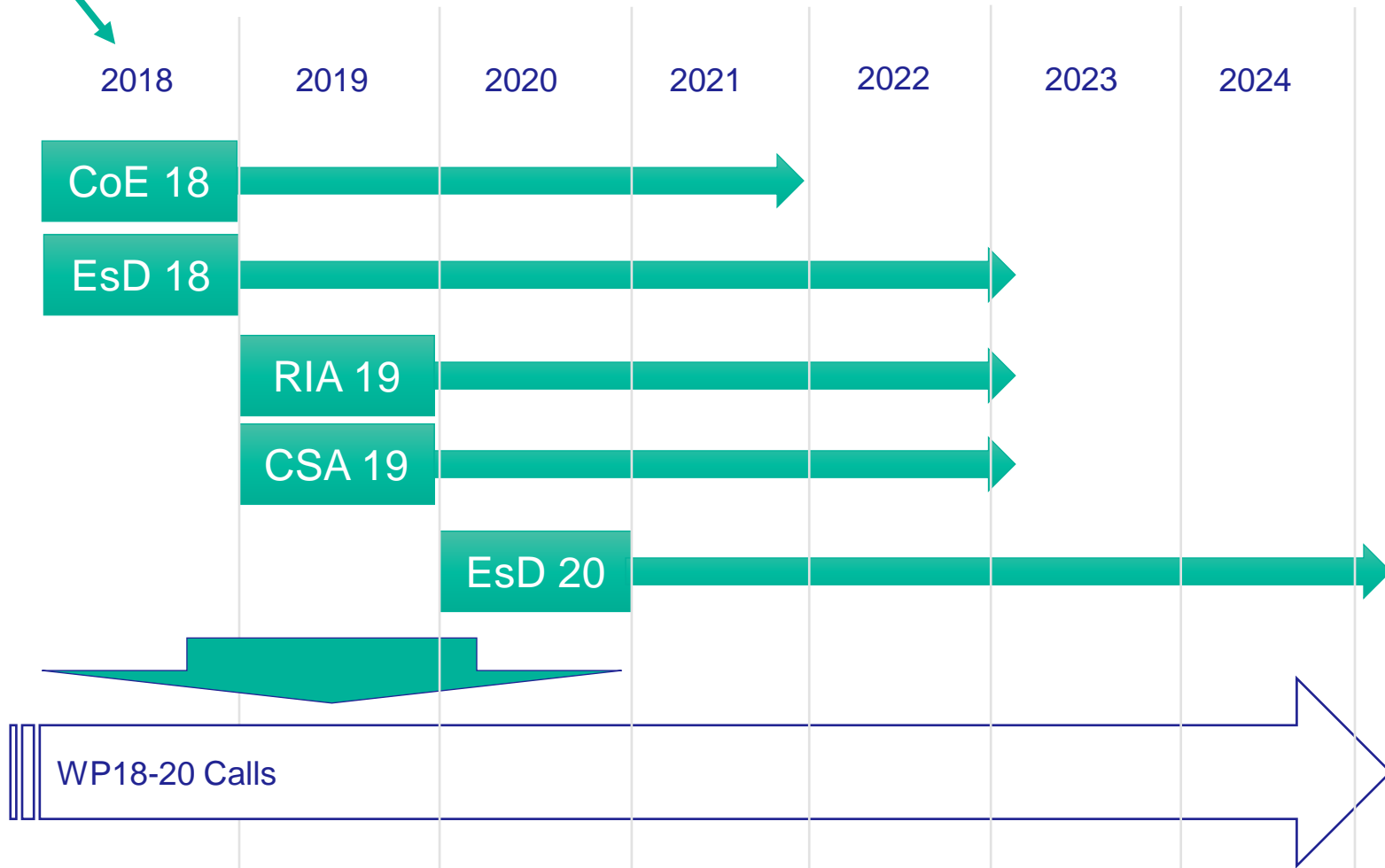


SRAs/WPs IN HORIZON 2020 TIMELINE

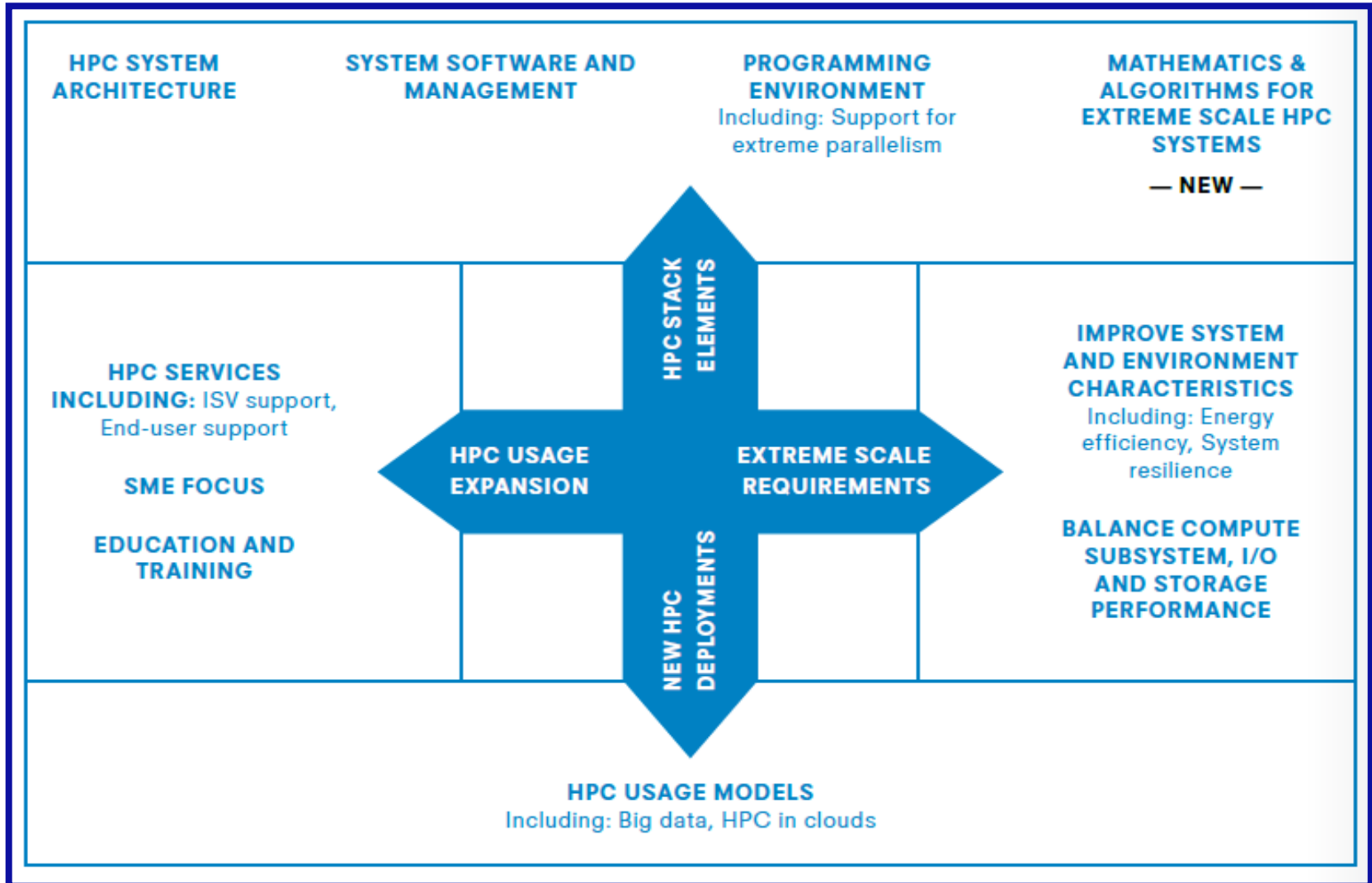




WP 18-20 COMPONENTS



MULTI-DIMENSIONAL SRA HPC MODEL



EXTREME-SCALE DEMONSTRATORS

HPC Centers

Participate in the co-design process
Manage system deployment
Operate
Validate and characterise the system

Technology Providers

Ensure the integration of the technologies
Perform the testing and quality/performance assurance
Perform the maintenance and service

1. Integrate results of R&D projects into fully integrated systems prototypes.
2. Establish proof-points for the readiness, usability and scalability of the technologies

Application owners

Define application requirements
Port and optimise applications

EsD 2018:

- **technology-advancements**
- designpoint: 500-1000 PF
- power eff.: 35kW/PFLOPS
- density: 1PF/rack
- I/O balanced design

EsD 2020:

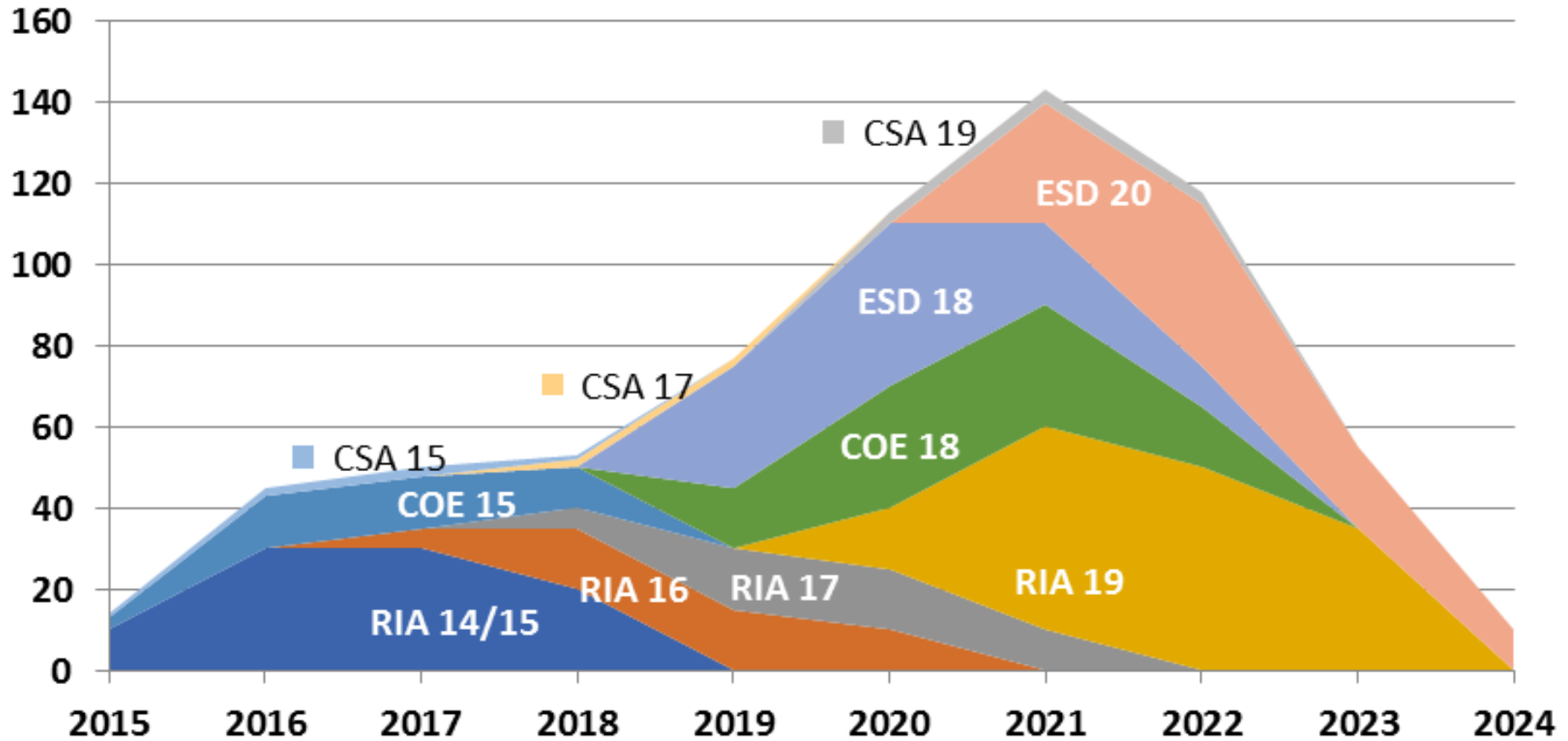
- technology: next generation
- **new deployment areas:**
 - HPDA / ML
 -

WP18-20 BUDGET RECOMMENDATIONS

Call-ID	Title	Total budget (M EUR)	Project sizes (M EUR)
ESD call 2018	Extreme scale Demonstrators	100	50
ESD call 2020		100	50
CoE call 2018	Centres of Excellence	90	6-8
RIA call 2019	Research and Innovation Actions	153	1) 15-20 (30) 2) 4-10
CSA call 2019	HPC ecosystem - CSA	7	7
		450	

H2020 HPC WORK PROGRAMME – DURATION/VALUES (EURO Ms)

Funding WP 14-20





STRATEGIC RESEARCH AGENDA (SRA)

Our Multi-Annual HPC Technology Roadmap

www.etp4hpc.eu/sra

SRA 3 ROADMAP IN 2017

- **March 20th:** Kickoff meeting at IBM IOT center in Munich
(SRA –workgroup leads, application owners, CoE, HiPeac, BDVA, EUROLAB-4-HPC, BDEC)
- **March 27th:** New SRA working groups in place (based on WP18-20 workgroup participants)
- **April:** Gather input from working groups (questions /recommendations)
- **May 18th:** EsD - Roundtable during HPC summit (Barcelona)
(FETHPC projects, CoE, HPC centers, system integrators, technology providers)
- **May 19th:** SRA-workgroup leaders' internal meeting (Barcelona)
- **June 22nd:** Workshop at ISC with industrial users (“how to benefit from EsDs?”)
- **April-June:** writing, interlock with workgroups
- **July:** integration, tuning, review
- **July 31st:** completion target
- **September 15th:** release and distribution after WP17 call closure

AGENDA SRA-3 KICKOFF MARCH 20TH 2017

- 10:30 Welcome and agenda review
- 10:45 New trends and requirements
 - 10:45-11:15 BDVA: Jim Kenneally
 - 11:15-11:45 CoE: Peter Bauer
 - 11:45-12:15 EXDCI-WP3: Stephane Requena
 - 12:15-12:45 EuroLab-4-HPC: Theo Ungerer
 - 12:45-13:15 HiPeac: Marc Durantou
 - Working Lunch
 - 14:00-14:30 BDEC: Mark Asch
 - 14:30-15:00 IPCEI-roadmap (Jean Gonnord)
- 15:00-16:00 SRA-structure: what is new, what to change?
- 16:00-17:00 Process, next meetings, next steps

ESD ROUNDTABLE AT ISC

Tentative agenda and setup (June 22nd):

- **Invitees:** One repr. from FETHPC projects, CoEs, Integrators, ETP4HPC workgroup leads
- **Main goal:**
 - update interested potential participants of EsD projects
 - level-set on general logistical / setup related issues
- **Agenda flow:**
 - FETHPC projects present anticipated deliverables offered for adoption in EsD projects
 - CoE present their suggestions for problems to solve & candidate applications
 - All: level set / recommendations going forward

SOME WORDS AT THE START OF SRA 3

- Since SRA 2 the HPC landscape in Europe changed :
 - European Open Cloud initiative
 - IPCEI
 - European Low-Power Microprocessor initiative
- The SRA is assumed to take these initiatives into account to be a relevant document for the HPC stakeholders in Europe
- We need an open, in-depth interlock with the EC and IPCEI
- We need to understand the technical roadmaps and the implementation plans



High Performance Computing

European timeline overview

Dr Gustav Kalbe

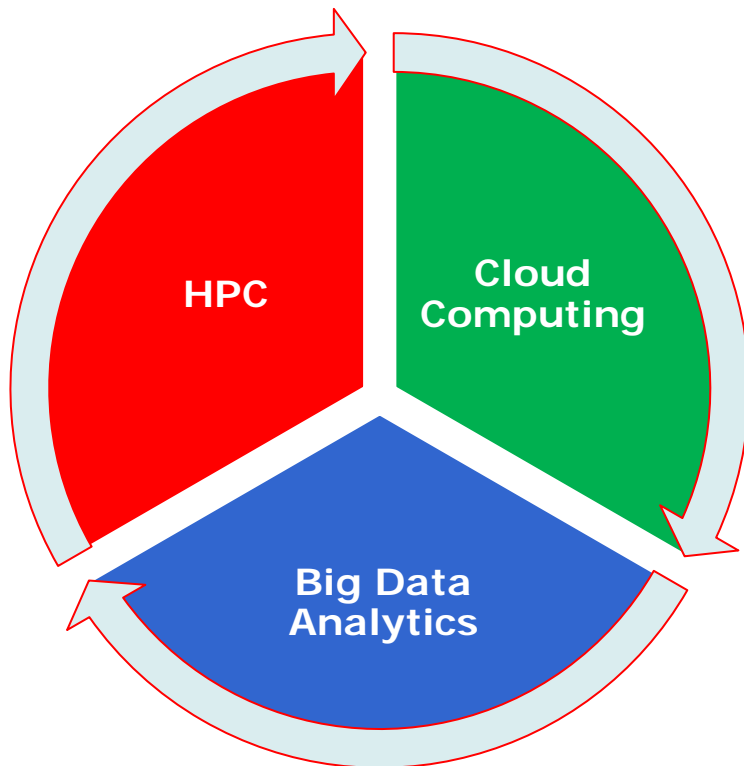
**Head of Unit – High Performance Computing & Quantum Technologies
DG CONNECT, European Commission**



- **Acquisition** (in 2020-2021) of 2 operational **pre-exascale** and (in 2022-2023) two full **exascale** machines (of which one based on European technology)
- **Interconnection and federation** of national and European HPC resources and creation of an HPC and Big Data service infrastructure facility
- **Demonstrating and testing** technology performance towards exascale through scientific & industrial compute-intensive applications

Aim: Build a world-class European High Performance Computing (HPC), Big Data (BDA) and Cloud Ecosystem

Enabled by the Convergence of 3 big technologies



- Major investments so far both at MS and EU level [FP7, H2020]
- Numerous research players (academia and industry)
- HPC and Big Data PPPs, PRACE, GEANT, etc.

HPC/EDI: EU investments



FET & LEIT Calls: technology development, integration, pilot test-beds and applications

- Technology development (low-power processor, SW, applications)
- Integrating and co-designing extreme scale systems

**HPC – Cloud – BDA
Ecosystem development**

Two pre-exascale

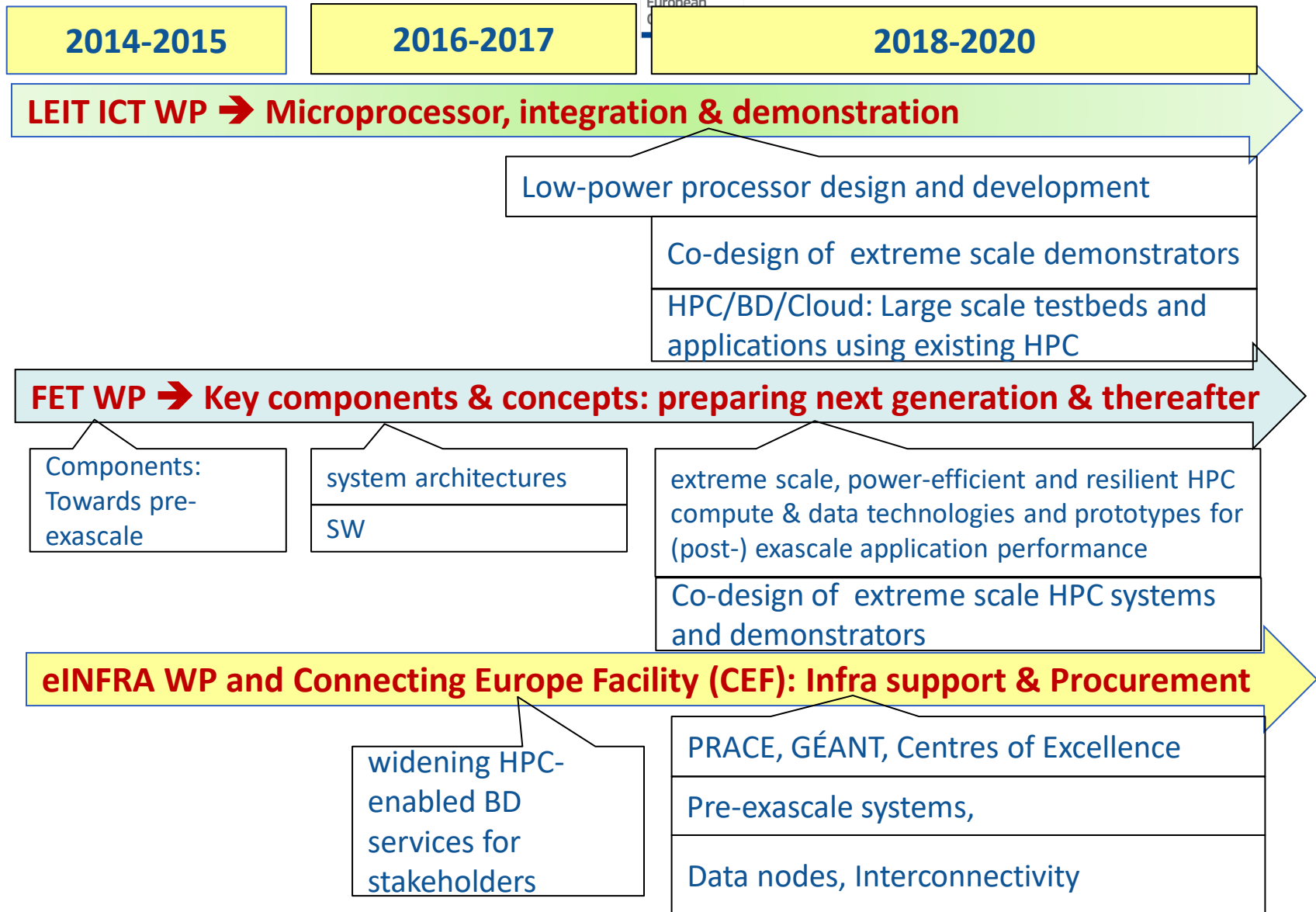
Two exascale

Infrastructure/CEF calls

- Centres of Excellence, Ecosystem development
- Procurement and services for EDI/HPC infrastructures (exascale, big data nodes, interconnection) and use widening



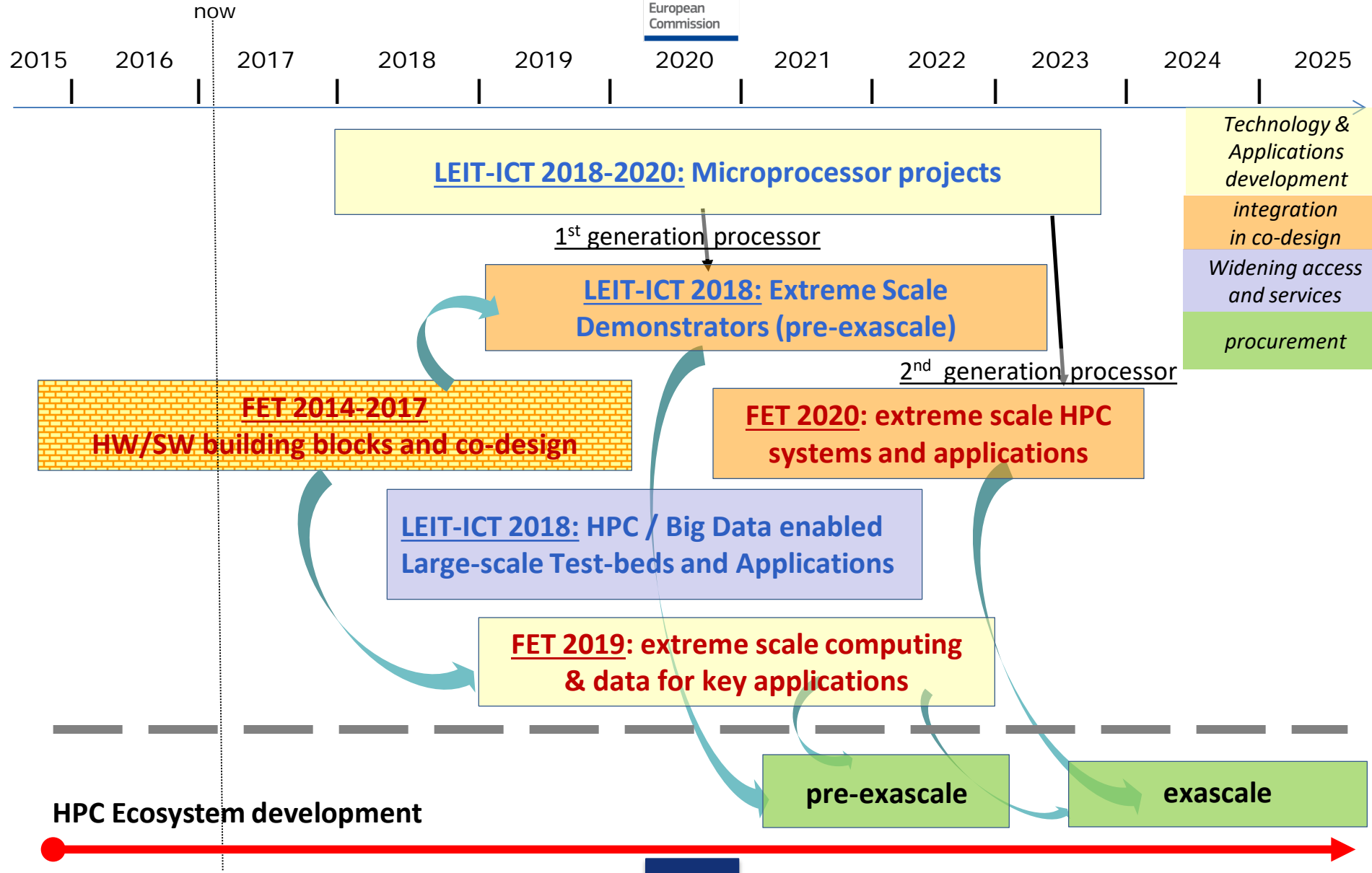
HPC/EDI in Horizon 2020 Work Programmes



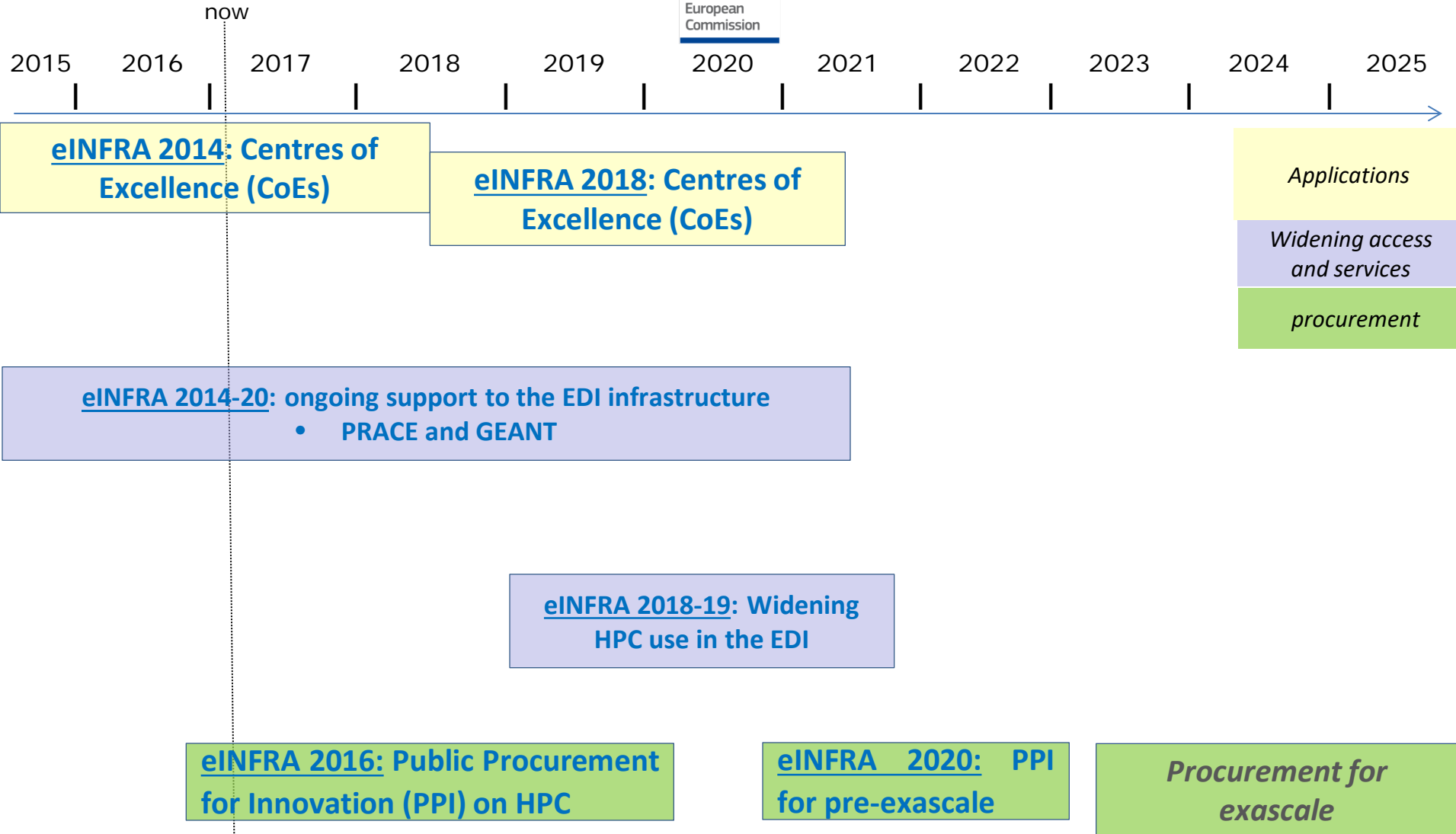
HPC timeline LEIT/FET (indicative)



subject to discussion with committees



HPC timeline eINFRA (indicative)





An articulated implementation to realise the political ambition

- *Clear roadmap and timeline*
- *Coordinated actions using all mechanisms of H2020*
- *Creating and covering the full HPC ecosystem*
 - Technology development
 - Co-design and integration
 - Applications and test-beds
 - HPC infrastructure development
 - Widening use of HPC
- *Further strong cooperation with MS*
- *Governance structure on HPC/EDI (Rome 23/03)*



THANK YOU!



DISCUSSION

LUNCH