EuroEXA

Co-designed Innovation and System for Resilient Exascale Computing in Europe: From Applications to Silicon

Presenter – Paul Carpenter
Barcelona Supercomputing Center
paul.carpenter@bsc.es

Leader WP2 Applications and Software Technical Manager, EuroEXA
Leader WP3 Enablement of Software Compute Node, ExaNoDe
EuroEXA project

- H2020 FETHPC-01-2016
- September 2017 – February 2021 (3.5 years)
- Budget €20 M
EuroEXA in context

Alliance of Multiple Projects, IP and Partners

Open Competitive Exercise Organised by the EU

EU Funding & Monitoring

Other Partners

EURO SERVER

ExaNoDe  ECOSCALE  ExaNeSt

arm

Additional IP

Paul Carpenter, EuroEXA & ExaNoDe
Co-designed Applications and Software Stack

21 Sep 2018
Co-design and demonstrate 1 PF+ testbed in operational environment

Three testbeds to be deployed at STFC, Daresbury

**Testbed 1**
50 nodes of ExaNeSt technology for software development

**Testbed 2**
~500 co-designed nodes and new infrastructure technologies to test scaling

**Testbed 3**
Test new node and processor technologies that will ultimately project to exascale

- **Mid 2018**
- **Early 2019**
- **2020**
Deliver available performance to full-scale production applications

- AVU-GSR
- Quantum Espresso
- SMURFF
- Neuromarketing
- NEMO
- Astronomy image classification
- NEST/DPSNN
- FRTM
- InfOli
- IFS
- LBM
- Alya
- GADGET
- LFRic

FLOPS

IOPS

Mem BW

Mem capacity
Co-design: Balance between compute resources and application demands

SoC cache sizes vs number of cores

- Xilinx Zynq UltraScale+ ZU9P for interconnect
- Xilinx Zynq UltraScale+ VU9P for acceleration
- ARM cores for control and non-accelerated code
EuroEXA full-scale exascale-class applications

- SLURM scheduler
- Allinea debug
- Aftermath monitor
- BeeGFS storage
- OpenStream
- OmpSs clusters and FPGA
- Co-design MPI
- Full MPI-3
- GPI
- UNIMEM API, OS kernel and firmware
- Xilinx tools
- Maxeler MaxJ
- OpenCL
- Accelerated libraries

Complete HPC software stack
Summary

• Co-design and demonstrate 1 PF+ testbed in operational environment
• Vision is exascale machine for Europe

• High performance for full-scale production applications
• Co-design led to SoC design choices and change in FPGA
• Complete software stack and optimized portable programming models
• Ongoing porting of applications to the architecture

• For more information, visit the BSC booth 2038
Backup
EuroEXA objectives

- Co-design and demonstrate 1 PF+ testbed in operational environment
- Build on foundation from EUROSERVER, ExaNoDe, ExaNeSt, ECOSCALE projects
- Global address space (UNIMEM) and FPGA compute acceleration
- Deliver available performance to full-scale production applications
- Achieve balance between compute resources and demands of applications