www.bsc.es

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

EXCELENCIA SEVERO OCHOA

An European "Flagship" project for HPC

ETP4HPC General Assembly

Prof. Mateo Valero
BSC Director

HPC is a global competition

"The country with the strongest computing capability will host the world's next scientific breakthroughs".

US House Science, Space and Technology Committee Chairman
Lamar Smith (R-TX)

Europe in the global HPC race

"Our goal is for Europe to become one of the top 3 world leaders in high-performance computing by 2020."

Jean Paul Juncker, 27 October 2015

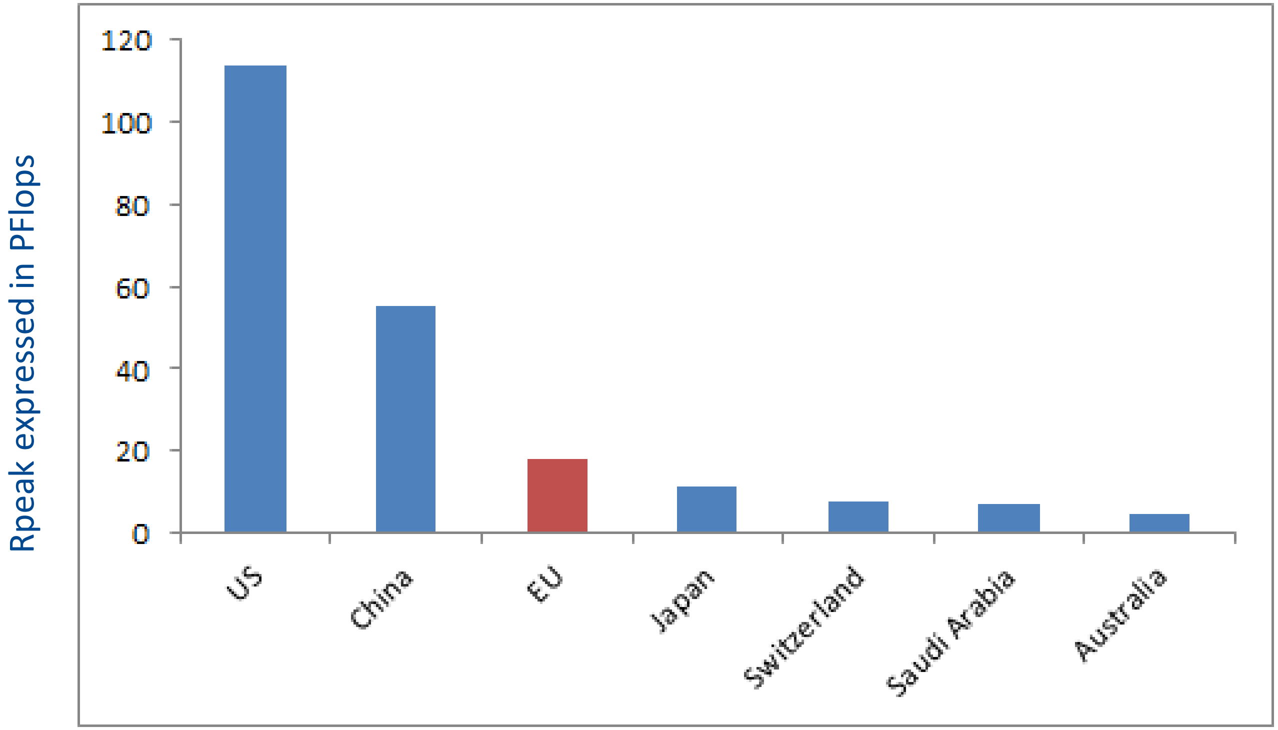
ICT 2015

BSC-CNS @BSC_CNS · 22 oct. 2015

"Europe needs research which is both excellent and relevant" Mateo Valero at #ICT2015 #HPC

5 3

Top 20 Supercomputers



Top 20 supercomputers

1. China
2. US
3. US
4. Japan
5. US
6. US
7. Switzerland
8. Germany
9. Saudi Arabia
10. US
11. Germany
12. US
13. US
14. US
15. US
16. US
17. Australia
18. US
19. Italy
20. US

Source: Top500 ranking, November, 2015

Worldwide HPC roadmaps

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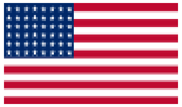


The White House
Office of the Press Secretary

For Immediate Release July 29, 2015

Executive Order -- Creating a National Strategic Computing Initiative

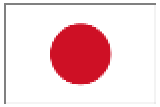
EXECUTIVE ORDER

\- - - - - - -

CREATING A NATIONAL STRATEGIC COMPUTING INITIATIVE

By the authority vested in me as President by the Constitution and the laws of the United States of America, and to maximize benefits of high-performance computing (HPC) research, development, and deployment, it is hereby ordered as follows:

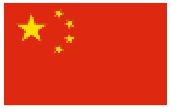
with domestic technology.



From K computer…

… to Post K

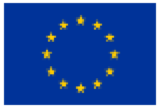
with domestic technology.



From Tianhe-2..

…to Tianhe-2A

with domestic technology.



IPCEI on HPC

From the PPP for HPC…

to future PRACE systems…

…with domestic technology ?

The US roadmap

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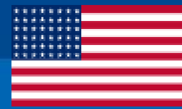
By FY18 deliver 3 different systems with at least 200 petaflops performance each

2 Power9 + NVIDIA (IBM) + 1 Intel + KNL (Intel + CRAY)

- NERSC has partnered with the Alliance for Computing at Extreme Scale (ACES) collaboration of Los Alamos National Laboratory (LANL) and Sandia National Laboratory (SNL) to form the Alliance for Application Performance at Extreme Scale (APEX).
- The focus of the APEX collaboration is on Application Performance of High Performance Computers and on meeting the mission needs of its partners and in pursuing Advanced Technology concepts.

The US roadmap



The White House

Office of the Press Secretary

For Immediate Release July 29, 2015

Executive Order -- Creating a National Strategic Computing Initiative

- Department of Energy = 285 million
- National Science Foundation = 33 million

Budget for FY2017 released in February 2016

- Department of Defense
- Intelligence Advanced Research Projects Activity - IARPA
- National Institute of Standards and Technology - NIST

Source: http://www.hpcwire.com/2016/02/12/obama-budget-reveals-new-elements-exascale-program/

The Exascale Computing Project (ECP)

- Starting this year, the ECP is initiated by DOE to:
- Develop a broad set of modeling and simulation applications that meet the requirements of the scientific, engineering, and nuclear security programs of the Department of Energy and the National Nuclear Security Administration (NNSA)
- Develop a **productive exascale capability in the US by 2023**, including the required software and hardware technologies
- Prepare two or more DOE Office of Science and NNSA facilities to house this capability
- Maximize the benefits of HPC for US economic competitiveness and scientific discovery

Source: Paul Messina ANL

ECP Scope

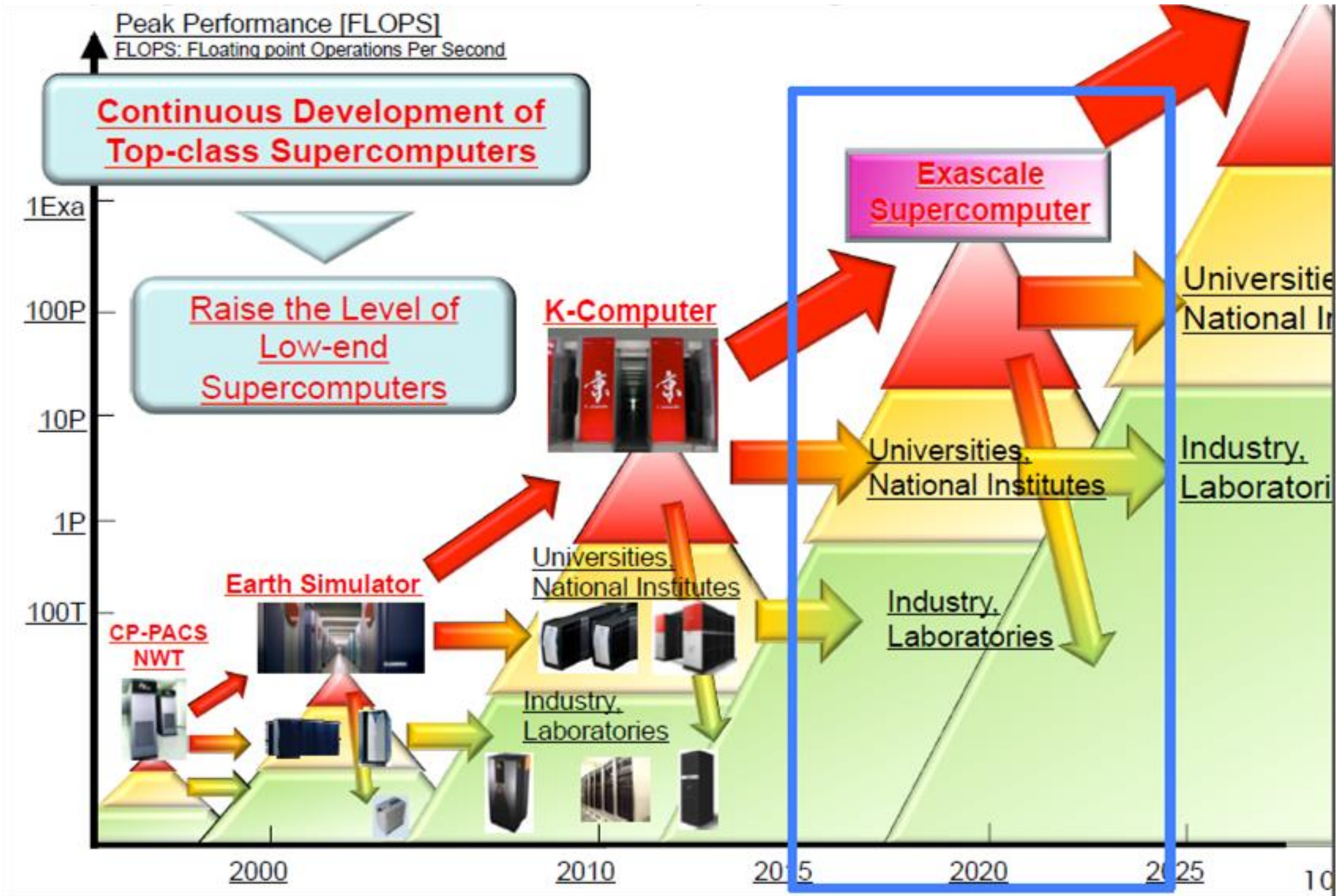
ECP will pursue a ten-year plan structured into four focus areas:

- **Application Development:** deliver scalable science and mission performance on a suite of ECP applications that are ready for efficient execution on the ECP exascale systems.
- **Software Technology:** enhance the software stack that DOE SC and NNSA applications rely on to meet the needs of exascale applications and evolve it to utilize efficiently exascale systems.
- **Conduct R&D:** on tools and methods that enhance productivity and facilitate portability.
- **Hardware Technology:** fund supercomputer vendors to do the research and development of hardware-architecture designs needed to build and support the exascale systems.
- **Exascale Systems:** testbeds, advanced system engineering development (NRE) by the vendors, incremental site preparation, and cost of system expansion needed to acquire capable exascale systems

Source: Paul Messina ANL

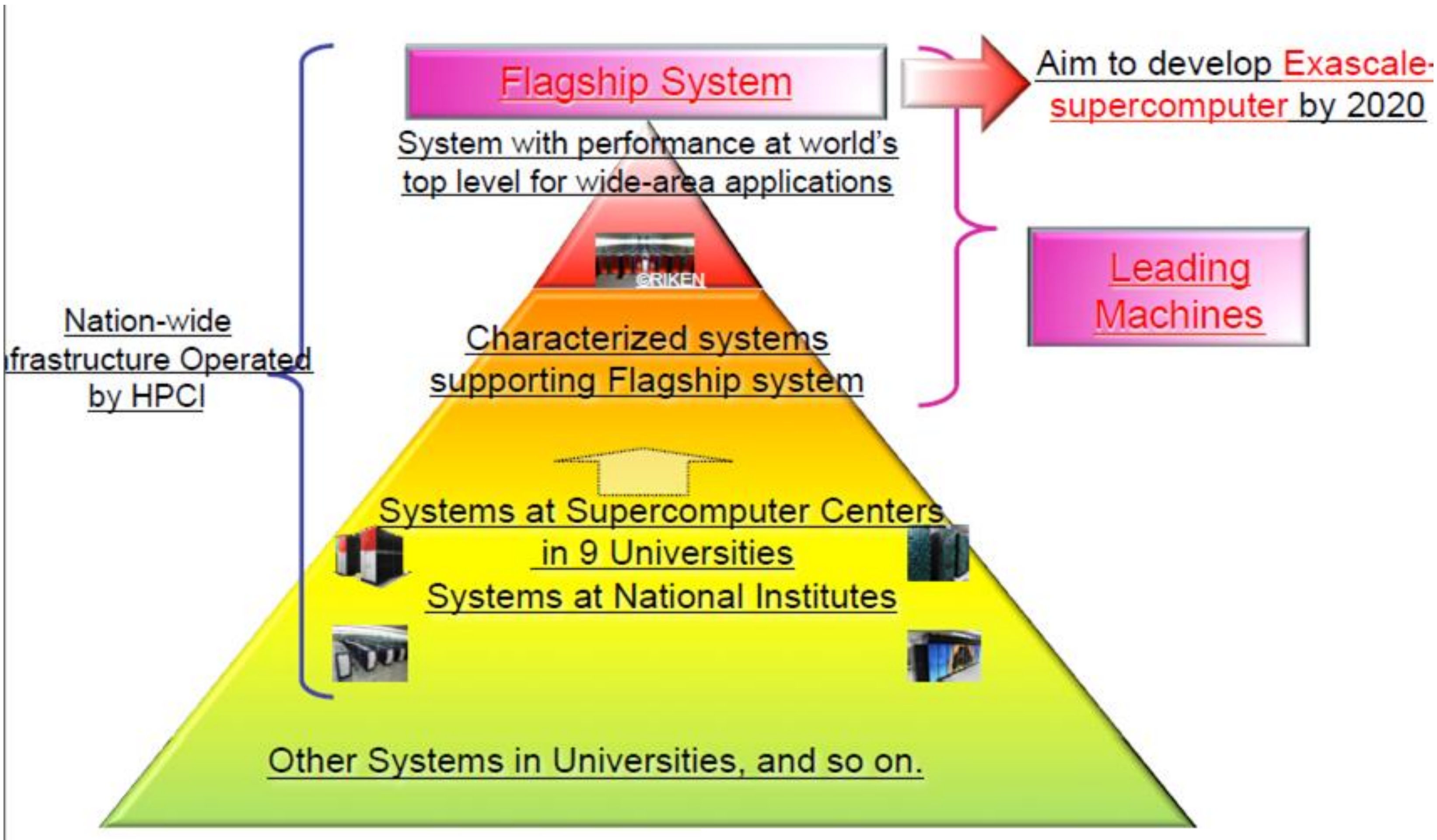
The Japanese roadmap

Continuous development of HPCI



Source: Yoshio Kawaguchi, "Japan's policy towards exascale computing", February 2014

Direction for development of next generation of supercomputers



Source: Yoshio Kawaguchi, "Japan's policy towards exascale computing", February 2014

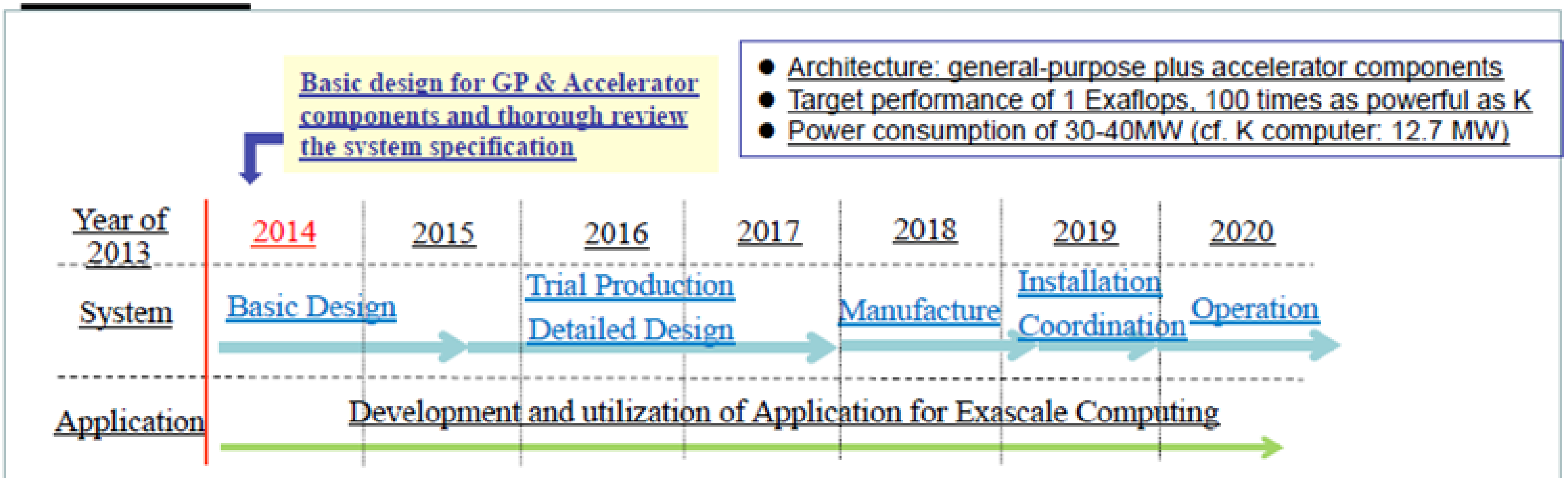
The Japanese roadmap

Japan Exascale System development

Outline:

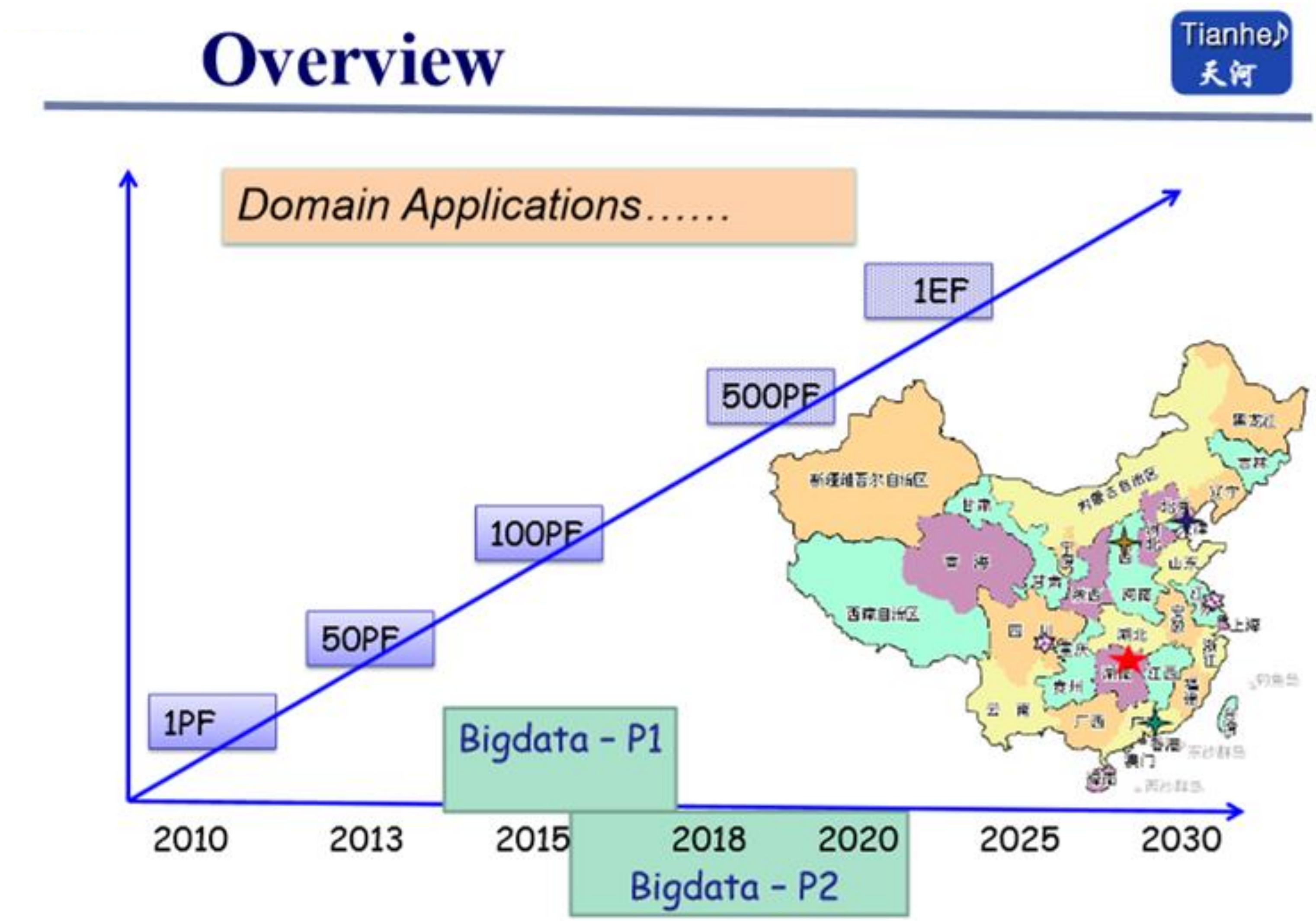
- Double-digits (higher)performance by 2020
- Push state of the art in power efficiency, scalability & reliability
- Enable unprecedented application capability
- AICS RIKEN in charge of exascale systems development
- Total project cost ca. JPY140 billion with about JPY 110 billion from the government's budget (JPY 1.2 billion for 2014)

Schedule:



Source: Yoshio Kawaguchi, "Japan's policy towards exascale computing", February 2014

The Chinese roadmap



Source: Yutong Lu, “Status o HPC and Big Data”

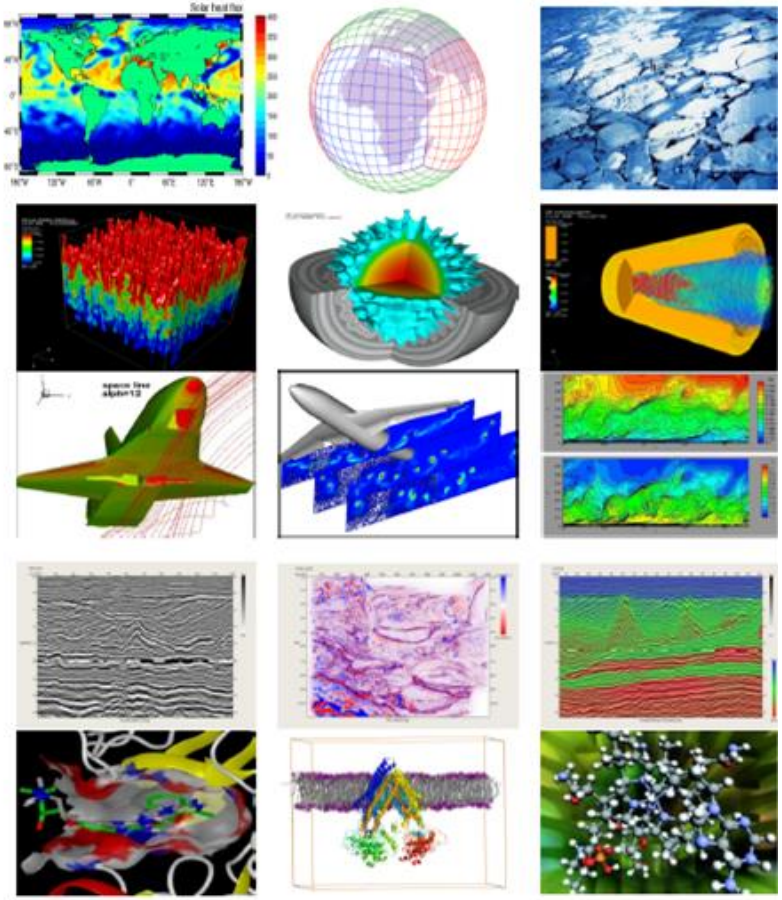
The Chinese roadmap

Domain Application

Tianhe 天河

Strategic domains

- Climate & Env.
- Fusion
- Aircraft Design
- Space & Cosmic
- Bio-Genomic
- Mechanical engineer
- New Material
- Electromagnetism
- Animation
- Oceanography



Source: Yutong Lu, “Status o HPC and Big Data”

The Chinese roadmap

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Funding System changing

NSFC
⟶ Basic algorithms and computable modeling for high performance scientific computing

- Novel computational methods and basic parallel algorithms
- Computable modeling for selected domains
- Implementation and verification of parallel algorithms by simulation

⟶ Network based research environment
⟶ Many-core parallel programming
⟶ Big data

MOST
⟶ Multiple Grand Projects

- Domain-centric

The 13th Five-Y Plan… (2016 - 2020)

- Infrastructure
- Software & Application
- International Joint project

Source: Yutong Lu, "Status o HPC and Big Data"

2012 - EC Communication on HPC

- EU needs independent access to HPC technologies, systems and services
- HPC funding should be doubled to 1.2 billion per year
- The EU HPC Industry should create ETP
- Centres of excellence for HPC applications should be established
- Hardware and software co-design centres should be set up to focus on the advancement of technologies, HPC resources, tools and methodologies

Key EU Policy developments in HPC

- Council Conclusions on High-Performance Computing (Competitiveness Council – 2013)
- Establishment of the European Technology Platform on High-Performance Computing (ETP4HPC - 2012) and Strategic Research Agenda on HPC (2013)
- Horizon 2020 programme including HPC Calls adopted (end of 2013)
- Public-Private Partnership with ETP4HPC (1st January 2014)

Source: Panagiotis Tsarchopoulos, "The European Supercomputing Research Programme", November 2015

The European roadmap

PRACE

ETP 4 HPC
THE EUROPEAN TECHNOLOGY PLATFORM FOR HIGH PERFORMANCE COMPUTING

HPC Infrastructure

HPC Technologies

700M€

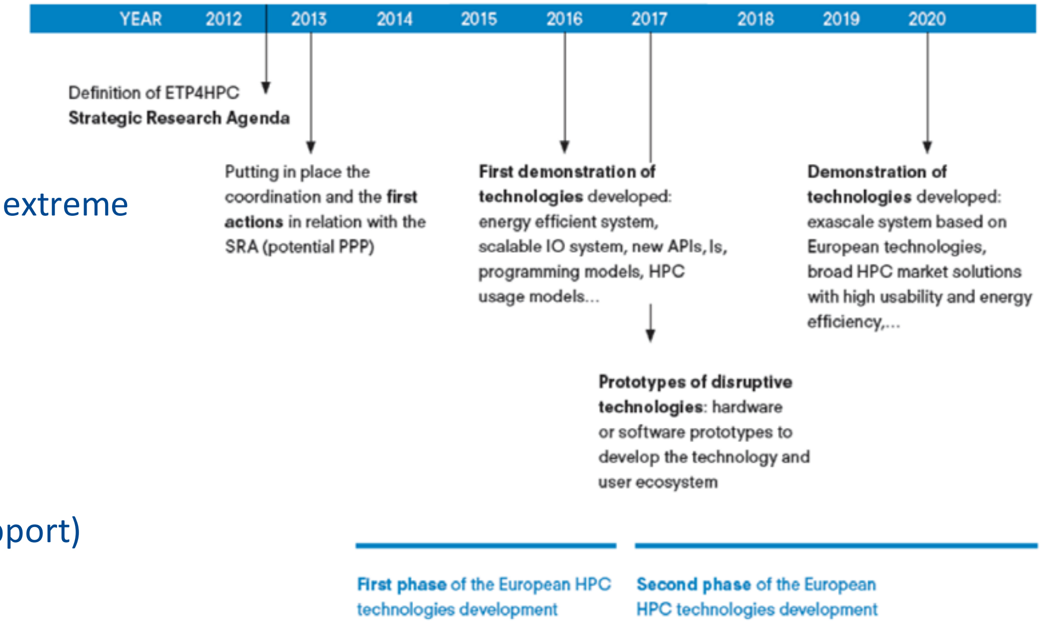
cPPP

esiwace
E CAM
pop
MaX
EoCoE
bioexcel
NOMAD
NOVEL MATERIALS DISCOVERY
CoeGSS
Centre of excellence for GLOBAL SYSTEMS SCIENCE

HPC Applications

The European roadmap

ETP4HPC



HPC stack elements

Programming environment (including support for extreme parallelism)
HPC system architecture
System software and management

HPC usage expansion

Usability
Affordability
HPC services (including: ISV support, end-user support)
SME focus
Education and training

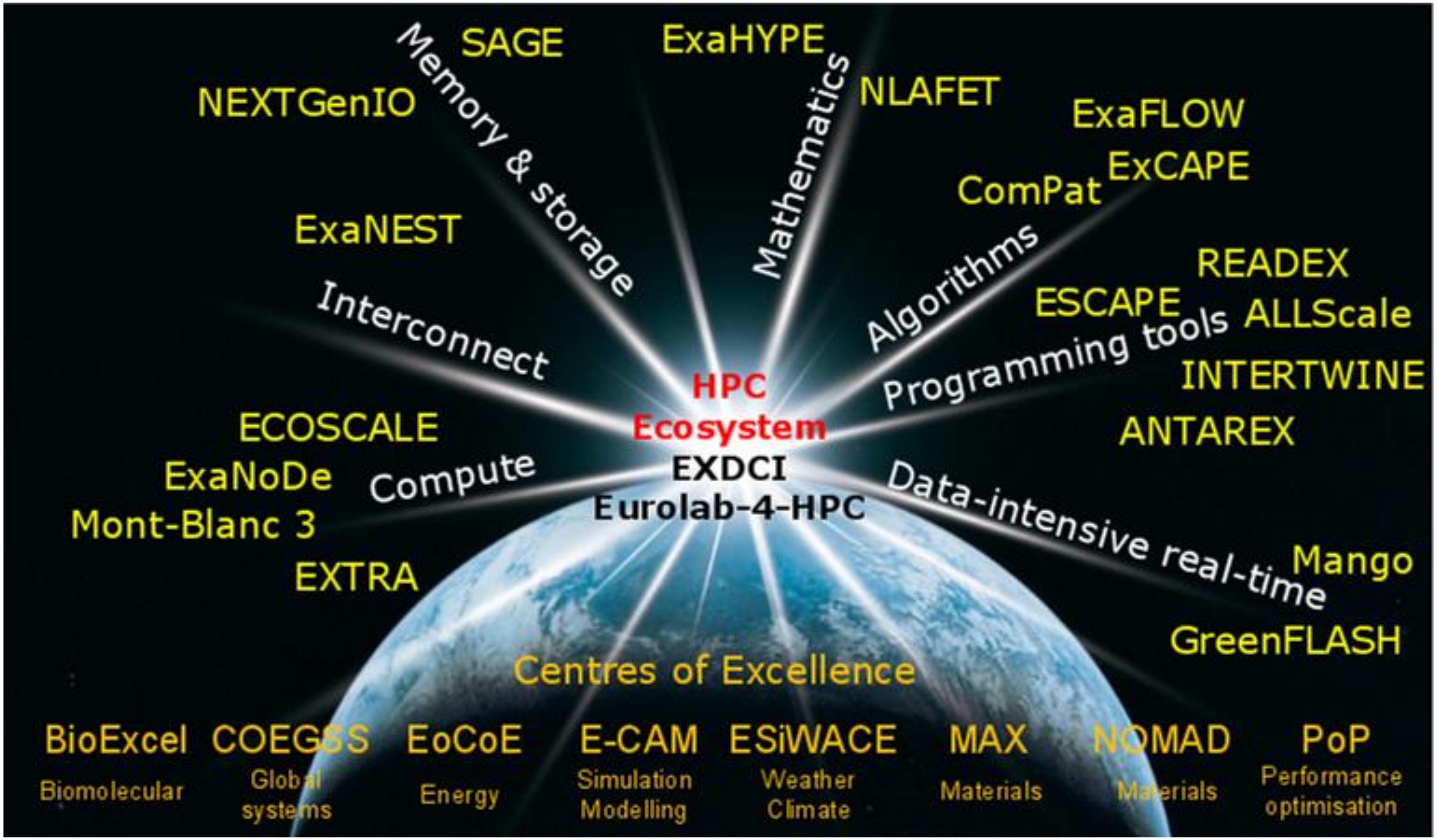
Extreme scale requirements

Improve system and environment characteristics (including energy efficiency, system resilience)
Balance compute subsystem, I/O and storage performance

New HPC developments

HPC usage models (including Big data, HPC in clouds)

Horizon 2020 and HPC



Source: Panagiotis Tsarchopoulos, "The European Supercomputing Research Programme", November 2015

The European H2020 FETHPC landscape

(1) Building FPGA-based prototypes (6 projects):

- MANGO: heterogeneous and custom accelerators emulated in Xilinx FPGAs
- Green FLASH: real-time telescope (E-ELT) controller using Altera FPGAs
- EXTRA: Maxeler reconfigurable architectures
- ECOSCALE: ARM + programming approach (UNILOGIC) for FPGAs
- ExaNoDe: ARM + Xilinx FPGAs
- ExaNEST: (ARM +) cooling and FPGA-based (prototype) interconnect

(2) Simulation-based SoC design (1 project):

- Mont-Blanc 3: design of HPC SoC based on ARM and accelerators

(3) Prototyping storage (2 projects)

- NEXTGenIO: prototype using Intel 3D Xpoint and Fujitsu integration
- SAGE: data-centric extreme data percipient storage

(4) Software only: algorithms, mathematics, or programming models (10 projects)

AllScale, INTERTWINE, ANTAREX, NLAFET, ComPat
ExaFLOW, ExCAPE, READEX, ExaHYPE, ESCAPE

January 2016 - IPCEI on HPC

European Commission › The Commissioners › Günther Oettinger › Blog ›

BLOG POST | By Günther Oettinger | 8 January 2016

Luxembourg launches Supercomputing Project

The Luxembourg government, together with France, Italy and Spain launched an "Important Project of Common European Interest" (IPCEI) on HPC and Big Data enabled applications.

"We are convinced that Europe has a unique opportunity to act and invest in the development and deployment of High Performance Computing (HPC) technology, Big Data and applications to ensure the competitiveness of its research and its industries".

Commissioner Oettinger, January 2016

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

- BSC-CNS objectives:
  - R&D in Computer, Life, Earth and Engineering Sciences
  - Supercomputing services to Spanish and EU researchers
  - PhD programme, technology transfer, public engagement

- BSC-CNS is a consortium that includes:

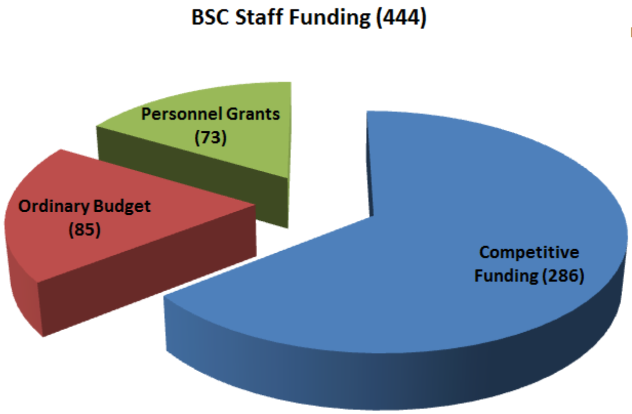
– Spanish Government	60%
– Catalonian Government	30%
– Universitat Politècnica de Catalunya (UPC)	10%

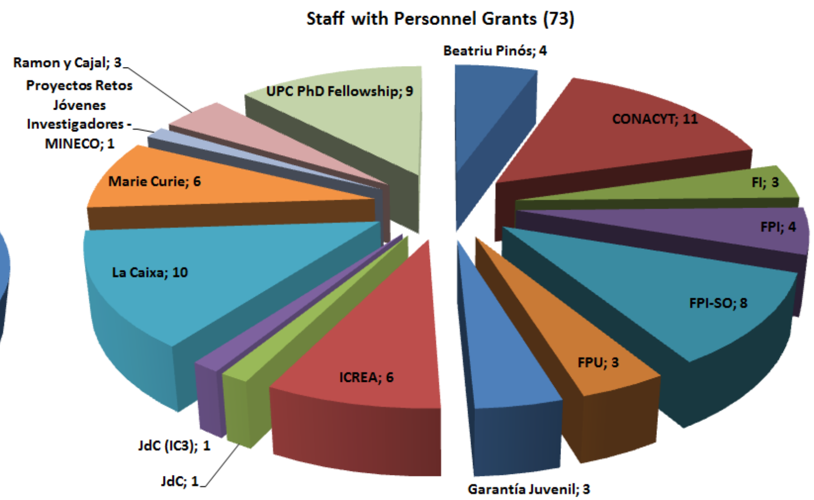
GOBIERNO DE ESPAÑA — MINISTERIO DE ECONOMÍA Y COMPETITIVIDAD

Generalitat de Catalunya
Departament d'Economia i Coneixement

UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH

- 444 people, 44 countries

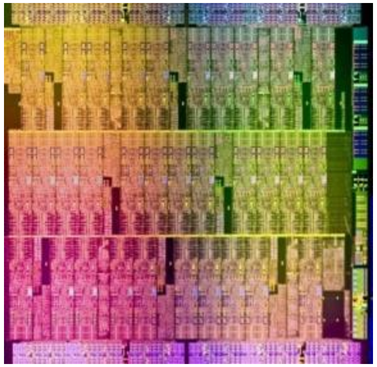




Mission of BSC Scientific Departments

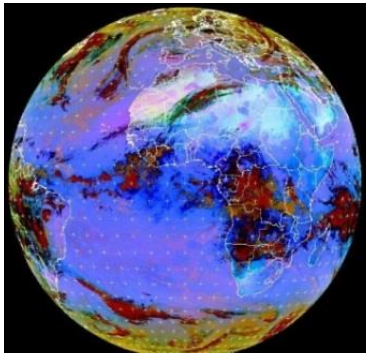
COMPUTER SCIENCES

To influence the way machines are built, programmed and used: programming models, performance tools, Big Data, computer architecture, energy efficiency



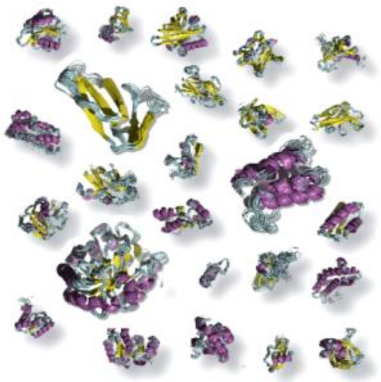
EARTH SCIENCES

To develop and implement global and regional state-of-the-art models for short-term air quality forecast and long-term climate applications



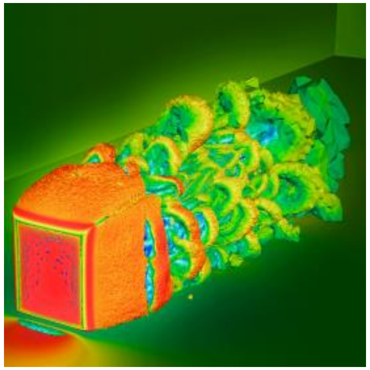
LIFE SCIENCES

To understand living organisms by means of theoretical and computational methods (molecular modeling, genomics, proteomics)



CASE

To develop scientific and engineering software to efficiently exploit super-computing capabilities (biomedical, geophysics, atmospheric, energy, social and economic simulations)



BSC & The Global IT Industry 2016

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IBM-BSC
Deep Learning Center

NVIDIA GPU
Center of Excellence

BSC-Microsoft Research Centre

Intel-BSC Exascale Lab

Mont-Blanc HPC Stack for ARM

Industrial applications

Pharmacelera · Dassault Aviation · Cenaero · Rolls Royce · Termo Fluids · Murex · AVL

Applications

GENCI · CINECA · Uni Graz · HLRS · University of Bristol

System software

ARM · ETH zürich · Inria · Bull atos technologies · Barcelona Supercomputing Center · Jülich Forschungszentrum

Hardware

ARM · Barcelona Supercomputing Center · Bull atos technologies · cea · UC Universidad de Cantabria

Seymour Cray Prize 2015

Mateo Valero

"Europe can develop an exascale machine with ARM technology"

Conclusions

1. US, Japan and China are all engaged in an Exascale race, since HPC has become strategic for science, industry, business and homeland security.
2. They have all similar and reasonable roadmaps supported by consequent budget allocation (typically 3-5 B USD in the next 10 years).
3. Europe has also expressed interest (Juncker, Oettinger, ICT2015, IPCEI etc…) in joining this race.
4. Europe through ETP4HPC, EXDCI and related activities has developed a comparable Exascale roadmap.
5. Adequate funding is unfortunately still missing. There are no additional funds behind the 700 M € in H2020.
6. If Europe doesn't want to be left behind and be dominated by foreign technology, it needs to develop an entire exascale stack from the processor all the way to the system and application software.
7. Europe (ARM, Linux…) has the competence and skills (see BSC long history in HPC architecture design) to engage in this race, provided adequate funding is made available.
8. A Flagship project (such as Human Brain or Graphene) needs to be launched and now!

HPC European strategy

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Centro Nacional de Supercomputación

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A window of opportunity is open!

It's time to invest in a *Flagship* project for Europe to succeed in HPC

Please all make your voice heard:
https://ec.europa.eu/futurium/en/content/fet-flagships

Maybe we need an AIRBUS consortium for HPC and Big Data www.bsc.es

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Thank you!

For further information please contact
mateo.valero@bsc.es

The Codesign Challenge

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

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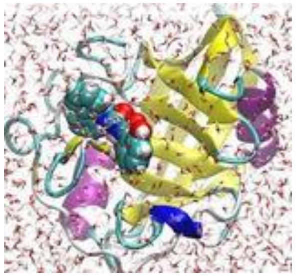
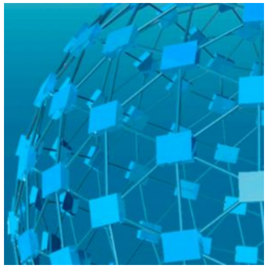
BSC participates



BioExcel

Centre of Excellence for Biomolecular Research (Led by KTH)



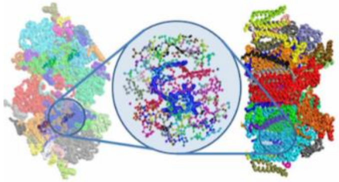
COEGSS

Center of Excellence for Global Systems Science (Led by Potsdam Uni)

BSC participates

EoCoE

Energy oriented Centre of Excellence (led by CEA)



E-CAM

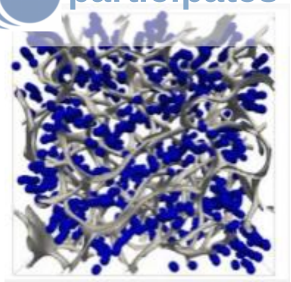
Software, training and consultancy in simulation and modelling (Uni College Dublin)

BSC participates

ESiWACE

Excellence in SImulation of Weather and Climate in Europe (Led by DKRZ)

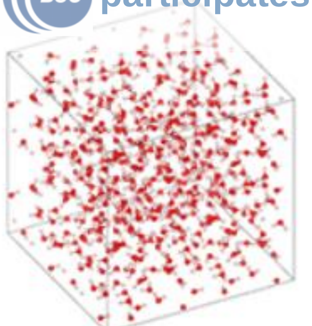
BSC participates



MAX

Materials design at the eXascale (Led by CNR)

BSC participates



NOMAD

The Novel Materials Discovery Laboratory (Led by Max Planck)

BSC leads

PoP

Performance Optimization and Productivity (Led by BSC)

Backup

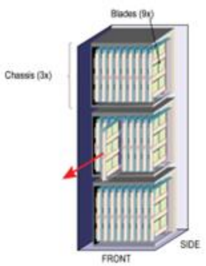
Backup slides

An ARM-based Exascale Prototype

February 24, 2016

EU Projects Unite on Heterogeneous ARM-based Exascale Prototype

Tiffany Trader



A trio of partner projects based in Europe – Exanest, Exanode and Ecoscale – are working in close collaboration to develop the building blocks for an exascale architecture prototype that will, as they describe, put the power of ten million computers into a single supercomputer. The effort is unique in seeking to advance the ARM64 + FPGA architecture as a foundational "general-purpose" exascale platform.

Funded for three years as part of Europe's Horizon2020 program, the partners are coordinating their efforts with the goal of building an early "straw man" prototype late this year that will consist of more than one-thousand energy-efficient ARM cores, reconfigurable logic, plus advanced storage, memory, cooling and packaging technologies.

Exanest is the project partner that is focused on the system level, including interconnection, storage, packaging and cooling. And as the name implies, Exanode is responsible for the compute node and the memory of that compute node. Ecoscale focuses on employing and managing reconfigurable logic as accelerators within the system.

Exanest

Manolis Katevenis, the project coordinator for Exanest and head of computer architecture at FORTH-ICS in Greece, explains that Exanest has set an early target of 2016 to build this "relatively-large" first prototype, comprised of at least one-thousand ARM cores.

He says, "We are starting early with a prototype based on existing technology because we want system software to be developed and applications to start being ported and tuned. For the remainder of the two years, there will be ongoing software development, plus research on interconnects, storage and cooling technologies. We also believe that there will be new interesting compute nodes coming out from our partner projects and we will use such nodes."

Exanest, Exanode and Ecoscale are seeking to advance the ARM64 + FPGA architecture as a foundational "general-purpose" exascale platform.

Objective: running real-world benchmarks and applications by 2018.

Source: http://www.hpcwire.com/2016/02/24/eu-projects-unite-exascale-prototype/?eid=330369000&bid=1322572/

The European H2020 FETHPC landscape

(1) Building FPGA-based prototypes
MANGO (UPV): heterogeneous and custom accelerators emulated in Xilinx FPGAs
Green FLASH (Observatoire de Paris): real-time telescope (E-ELT) controller using Altera FPGAs
EXTRA (Ghent): Maxeler reconfigurable architectures
ECOSCALE (TSI Crete, Iakovos): programming approach (UNILOGIC) for FPGAs
ExaNoDe [Cordis] (CEA): Xilinx FPGAs [BSC: Paul Carpenter]
Main activity is an FPGA-based prototype: http://www.hpcwire.com/2016/02/24/eu-projects-unite-exascale-prototype/
Ongoing work on 3D interposer integration, but no indication that it is European chiplets
ExaNEST (FORTH): cooling and FPGA-based (prototype) interconnect
(2) Simulation-based SoC design
Mont-Blanc 3 (Bull) [BSC: Filippo Mantovani]
SoC design using simulation
No actual SoC in the project
(3) Prototyping (non-European) storage
NEXTGenIO (EPCC): Intel and Fujitsu + 3D XPoint [BSC: Toni Cortes]
Prototype using Intel 3D Point built by Fujitsu: not European
SAGE (Seagate): data-centric extreme data storage “percipient storage"
Mostly software to tiered object-based storage: Seagate storage and Bull compute
(4) Software only: algorithms, mathematics, or programming models
AllScale (Innsbruck)
INTERTWINE (EPCC) [BSC: Viçenc Beltran]
ANTAREX (Politecnico di Milano)
NLAFET (Umea, Bo Kagstrom)
ComPat (U. Van Amsterdam)
ExaFLOW (KTH)
ExCAPE [Cordis] (IMEC)
READEX (TU Dresden)
ExaHYPE (TU Munich)
ESCAPE (ECMWF)