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Mont-Blanc work
Past, present & future

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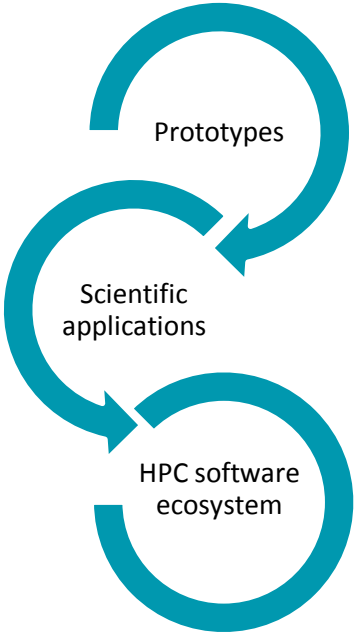
This project has received funding from the European Union's Horizon 2020 research and innovation program under grant agreement n° 671697

Mont-Blanc 3 key objectives

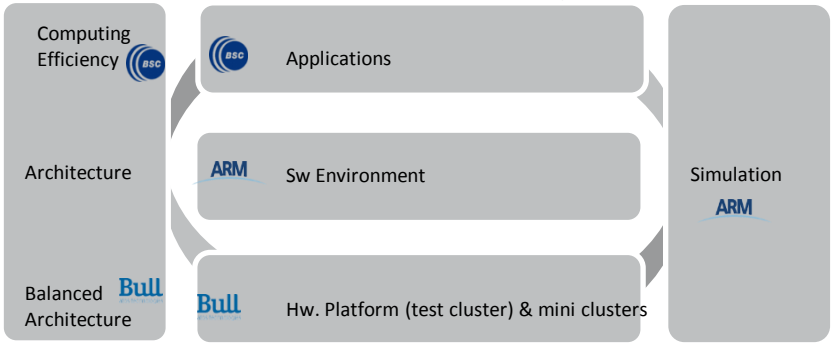
- **Design a compute node based on ARM architecture for a pre-exascale system**
  - Well balanced : Memory, Interconnect, IO
  - Simulation will be used to evaluate the options on applications
- **Evaluate new high-end ARM core and accelerator, and assess different options for compute efficiency**
  - Heterogeneous cores, new option for VPU, high performance core
  - Some assessment with existing solutions will be done using applications
  - One key idea : prepare to transform applications from being latency limited to throughput limited
- **Develop the software ecosystem needed for market acceptance of ARM solutions**



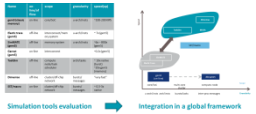
Our vision:

- **One single solution cannot optimally fit the needs of all HPC apps**
  - however economical efficiency requires generic solutions
  - need for an architecture flexible enough to permit and facilitate adaptation
- **Need to allow « good independence » of HPC app from underneath hw**
  - need therefore to
    - provide programmers with the right programming paradigms
    - work hard on processor performance
    - & propose evolution path for legacy applications
  - kind of “loose coupling” model between apps & platform developments
    - SVE’s vector-length agnosticism is a good example

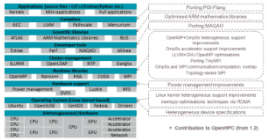
Anticipated technologies (hw/sw/methodology)



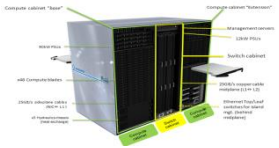
- Multiscale simulation methodology



- Software ecosystem



- Nextgen SoC requirements & design
- Global system architecture



More has to be done

(Provided)

- ✓ Nextgen SoC requirements & design
- ✓ Multiscale simulation methodology
- ✓ Software stack
- ✓ Global system architecture

Needed (non exhaustive list)

- ➔ SoC procurement
- ➔ Accelerators
- ➔ Data storage & mgt enhancement
- ➔ Enhanced programming models
- ➔ A committed set of use cases
- ➔ …

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EsD perspective

- **We (collectively) have to deliver, and to be user-oriented**
  (applications, reliability, ease of use …)

- **It is a matter of**
  - cooperation
  - technological choices (value added, maturity, complementarity ...)
  - integration
  - co-design

- **Exascale is a collective journey**
  - we’re probably just in the middle

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Thank you for your attention

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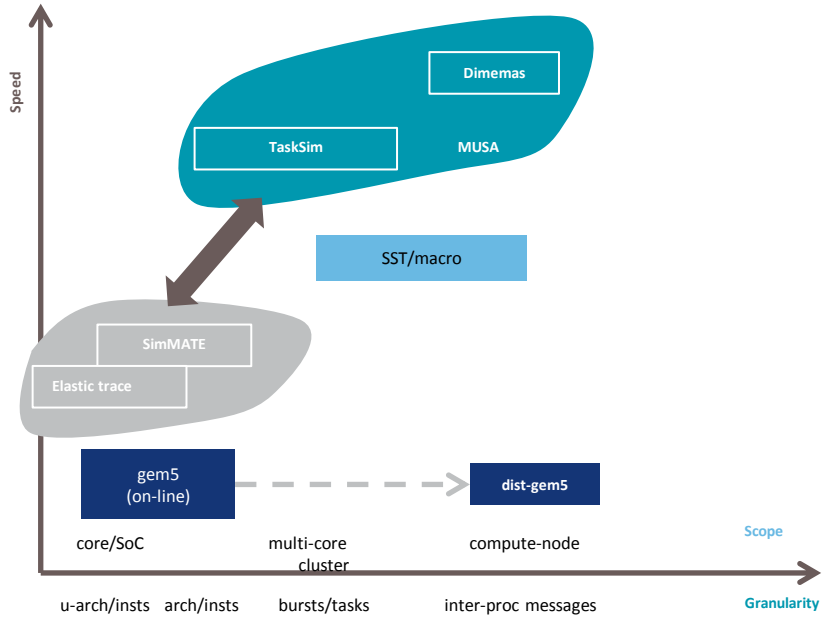
Backup slides

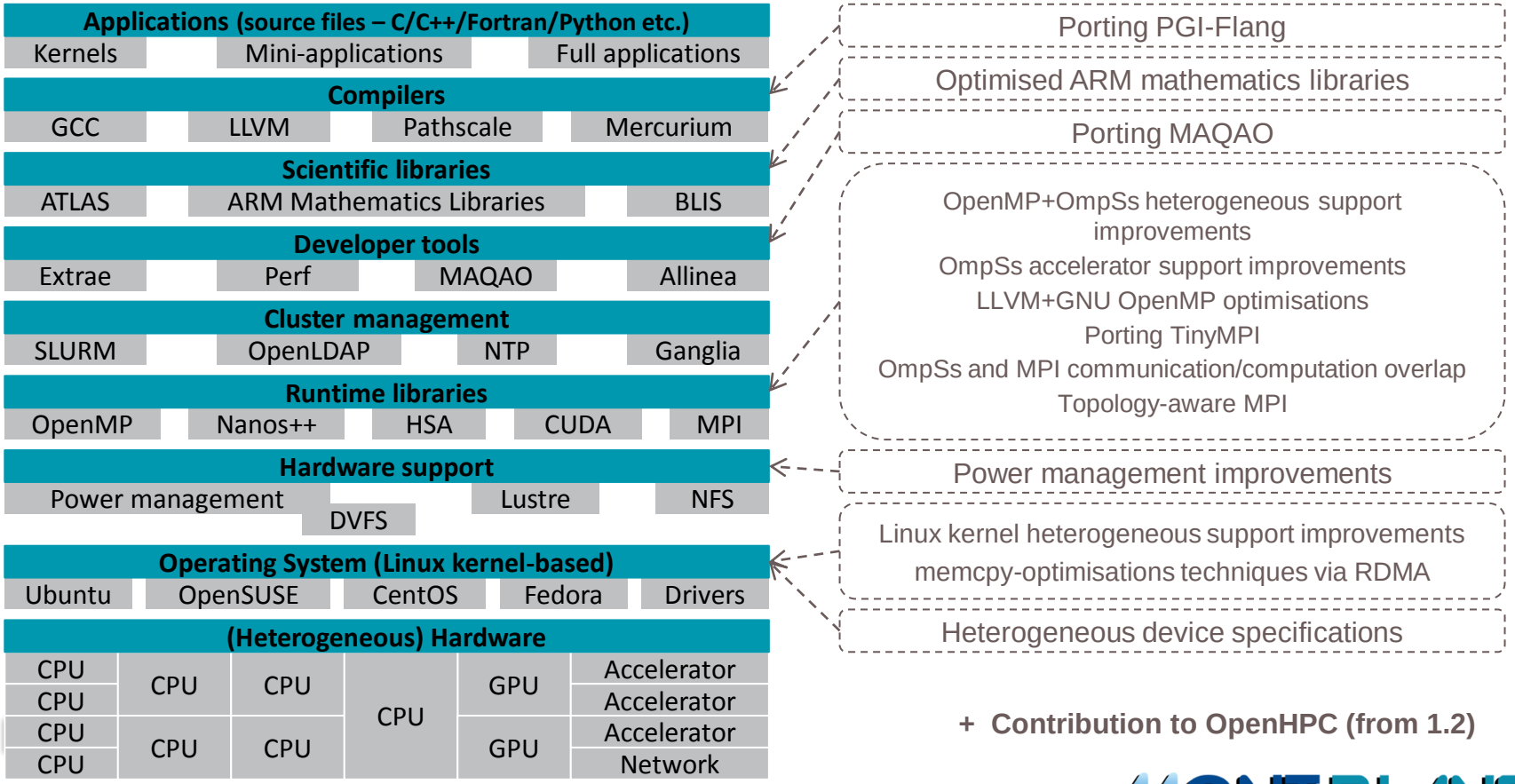
Name	on-line/offline	scope	granularity	speed(up)
gem5 (classic memory)	on-line	core/SoC	u-arch/insts	~100-200 KIPS
Elastic trace (gem5)	off-line	interconnect/memory system	u-arch/insts	~ 7x (gem5)
SimMATE (gem5)	off-line	memory system	u-arch/insts	~6x – 800x (gem5)
Garnet (gem5)	on-line	interconnect		~0.2x (gem5)
TaskSim	off-line	compute node/task scheduler	arch/tasks	~ 10x native (burst) ~20x gem5 (memory)
Dimemas	off-line	cluster/off-chip network	bursts/ messages	"very fast"
SST/macro	on-line	cluster/off-chip network	bursts/ messages	~ 0.3-3x native



Simulation tools evaluation

Integration in a global framework

HPC ARM Software Stack



+ Contribution to OpenHPC (from 1.2)

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Integration in industrial design (Bull sequana island)