ETP 4 HPC SRA

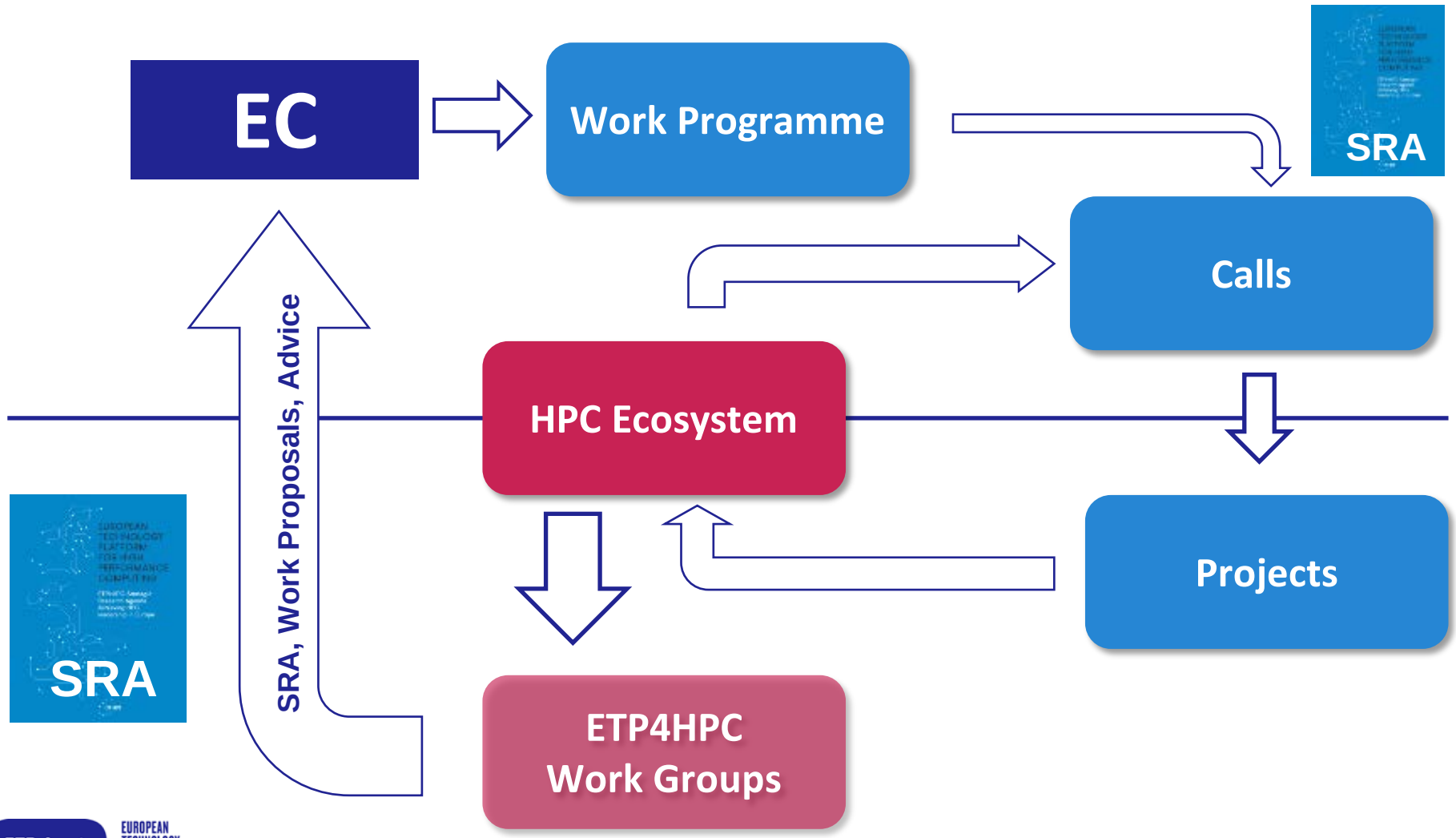
HIGH PERFORMANCE COMPUTING FOR EUROPE

WORKPROGRAMME 2018-2020 RECOMMENDATIONS

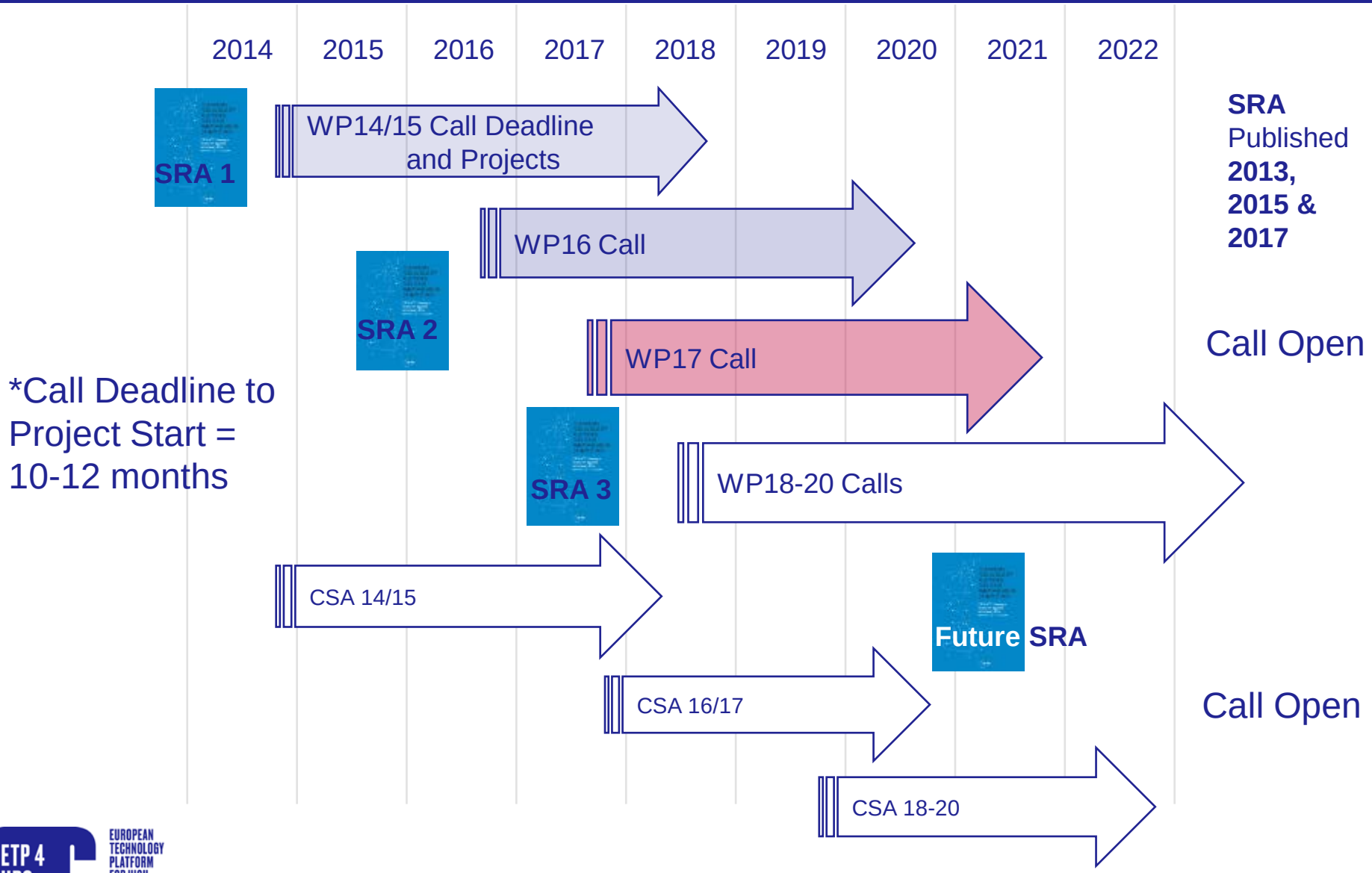
Our Multi-Annual HPC Technology Roadmap

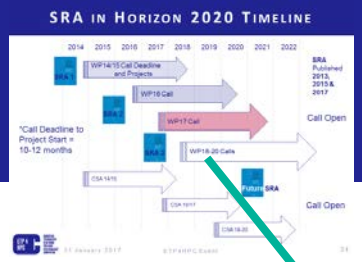
www.etp4hpc.eu/sra

SRAs and WPs: the Flow



SRAs/WPs in Horizon 2020 Timeline





WP 18-20 COMPONENTS

2018 2019 2020 2021 2022 2023 2024

CoE 18

EsD 18

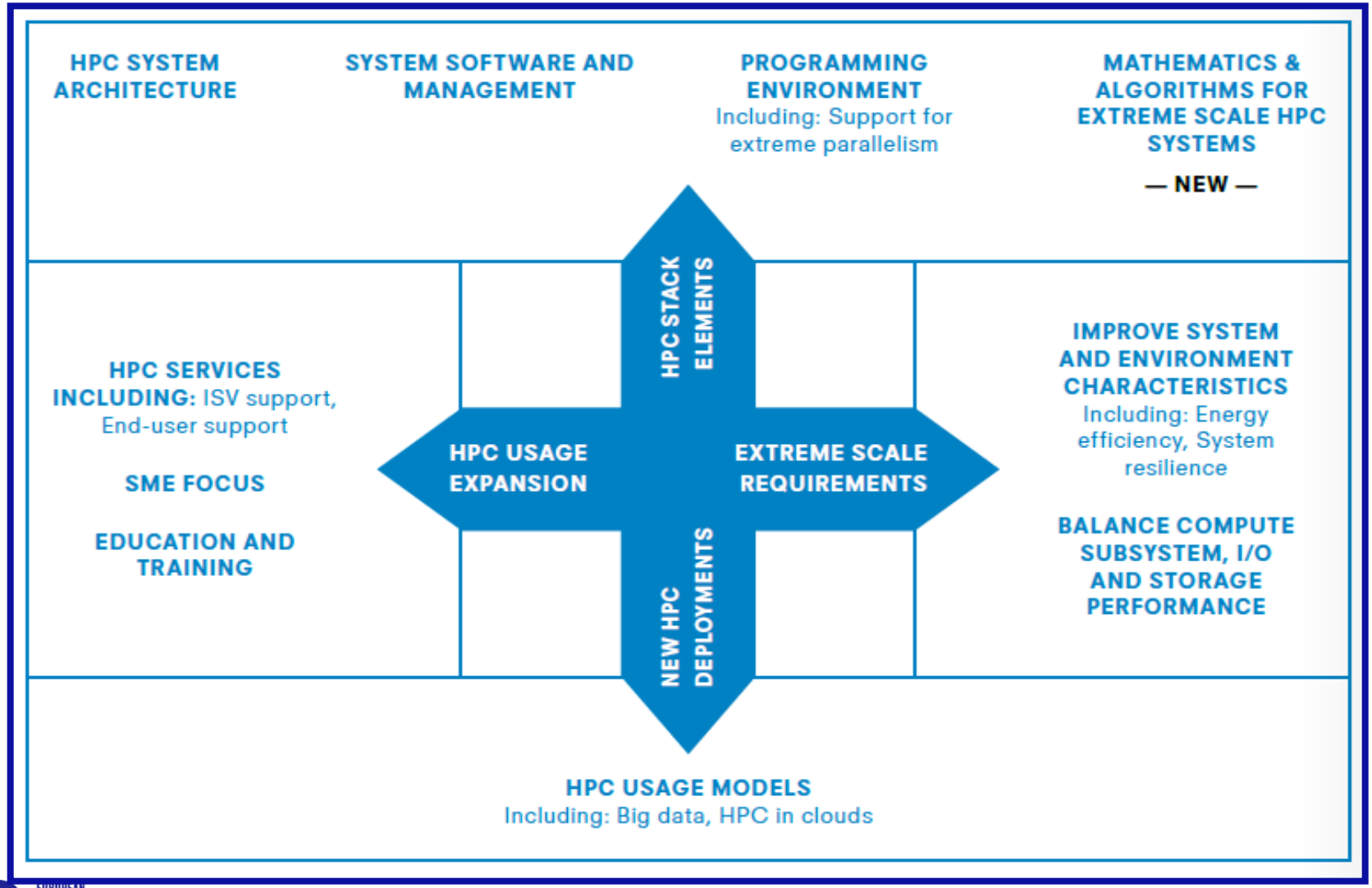
RIA 19

CSA 19

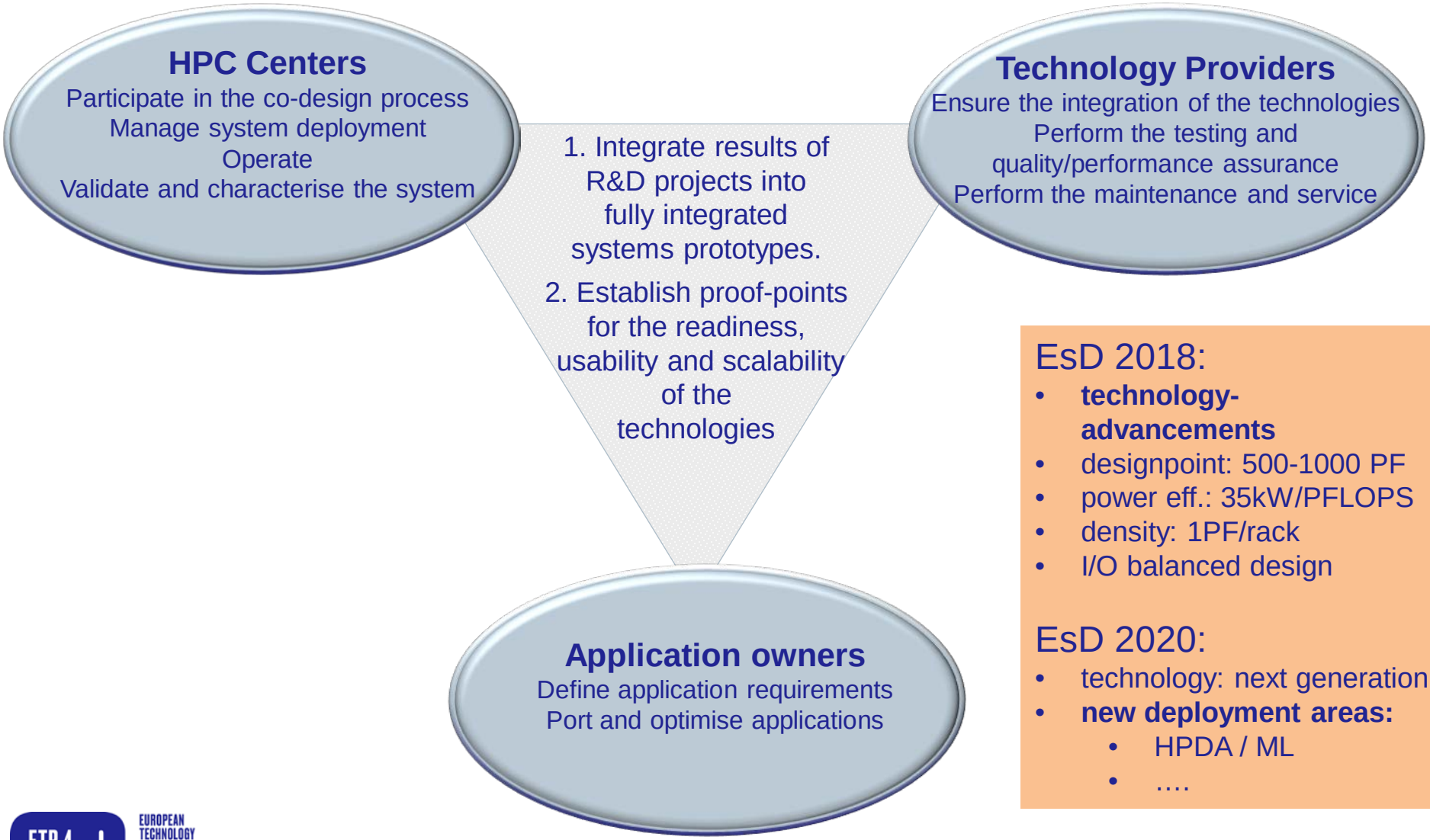
EsD 20

WP18-20 Calls

MULTI-DIMENSIONAL SRA HPC MODEL



EXTREME-SCALE DEMONSTRATORS



EsD 2018:

- **technology-advancements**
- designpoint: 500-1000 PF
- power eff.: 35kW/PFLOPS
- density: 1PF/rack
- I/O balanced design

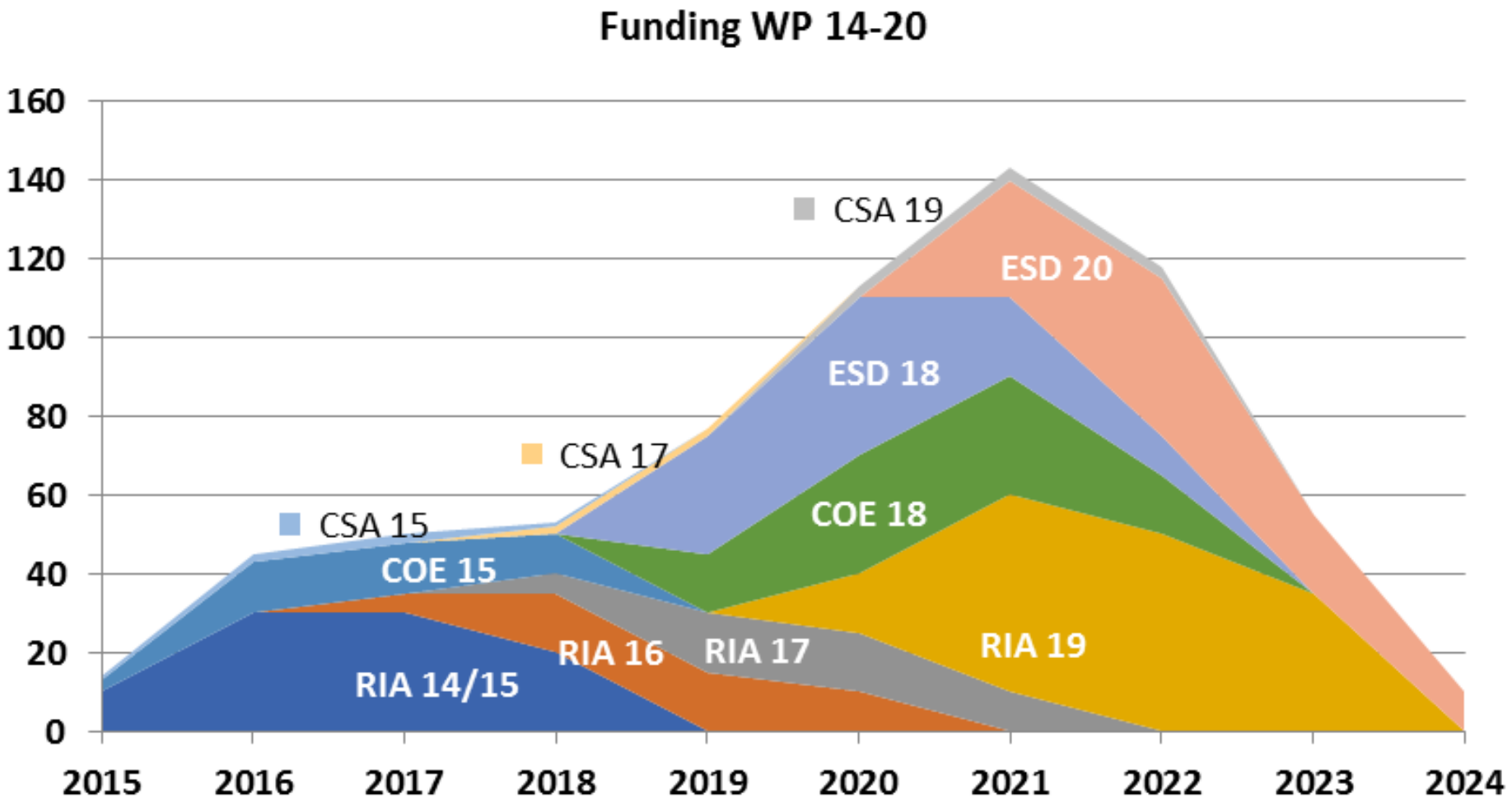
EsD 2020:

- technology: next generation
- **new deployment areas:**
  - HPDA / ML
  - ….

WP18-20 Budget recommendations

Call-ID	Title	Total budget (M EUR)	Project sizes (M EUR)
ESD call 2018 ESD call 2020	Extreme scale Demonstrators	100 100	50 50
CoE call 2018	Centres of Excellence	90	6-8
RIA call 2019	Research and Innovation Actions	153	1) 15-20 (30) 2) 4-10
CSA call 2019	HPC ecosystem - CSA	7	7
		450	

H2020 HPC Work Programme – Duration/Values (Euro Ms)



ETP 4 HPC SRA

HIGH PERFORMANCE COMPUTING FOR EUROPE

STRATEGIC RESEARCH AGENDA (SRA)

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SRA 3 ROADMAP IN 2017

- **March 20th**: Kickoff meeting at IBM IOT center in Munich

  (SRA –workgroup leads, application owners, CoE, HiPeac, BDVA, EUROLAB-4-HPC, BDEC)
- **March 27th**: New SRA working groups in place (based on WP18-20 workgroup participants)
- **April**: Gather input from working groups (questions /recommendations)
- **May 18th**: EsD - Roundtable during HPC summit (Barcelona)

  (FETHPC projects, CoE, HPC centers, system integrators, technology providers)
- **May 19th**: SRA-workgroup leaders' internal meeting (Barcelona)
- **June 22nd**: Workshop at ISC with industrial users ("how to benefit from EsDs?")
- **April-June**: writing, interlock with workgroups
- **July**: integration, tuning, review
- **July 31st**: completion target
- **September 15th**: release and distribution after WP17 call closure

Agenda SRA-3 kickoff March 20th 2017

- 10:30 Welcome and agenda review
- 10:45 New trends and requirements
  - 10:45-11:15 BDVA: Jim Kenneally
  - 11:15-11:45 CoE: Peter Bauer
  - 11:45-12:15 EXDCI-WP3: Stephane Requena
  - 12:15-12:45 EuroLab-4-HPC: Theo Ungerer
  - 12:45-13:15 HiPeac: Marc Duranton
  - Working Lunch
  - 14:00-14:30 BDEC: Mark Asch
  - 14:30-15:00 IPCEI-roadmap (Jean Gonnord)
- 15:00-16:00 SRA-structure: what is new, what to change?
- 16:00-17:00 Process, next meetings, next steps

ESD Roundtable at ISC

Tentative agenda and setup (June 22nd):

- Invitees: One repr. from FETHPC projects, CoEs, Integrators, ETP4HPC workgroup leads
- Main goal:
  - update interested potential participants of EsD projects
  - level-set on general logistical / setup related issues
- Agenda flow:
  - FETHPC projects present anticipated deliverables offered for adoption in EsD projects
  - CoE present their suggestions for problems to solve & candidate applications
  - All: level set / recommendations going forward

Some words at the Start of SRA 3

- Since SRA 2 the HPC landscape in Europe changed :
  - European Open Cloud initiative
  - IPCEI
  - European Low-Power Microprocessor initiative
- The SRA is assumed to take these initiatives into account to be a relevant document for the HPC stakeholders in Europe

➢ We need an open, in-depth interlock with the EC and IPCEI

➢ We need to understand the technical roadmaps and the implementation plans

High Performance Computing

European timeline overview

Dr Gustav Kalbe

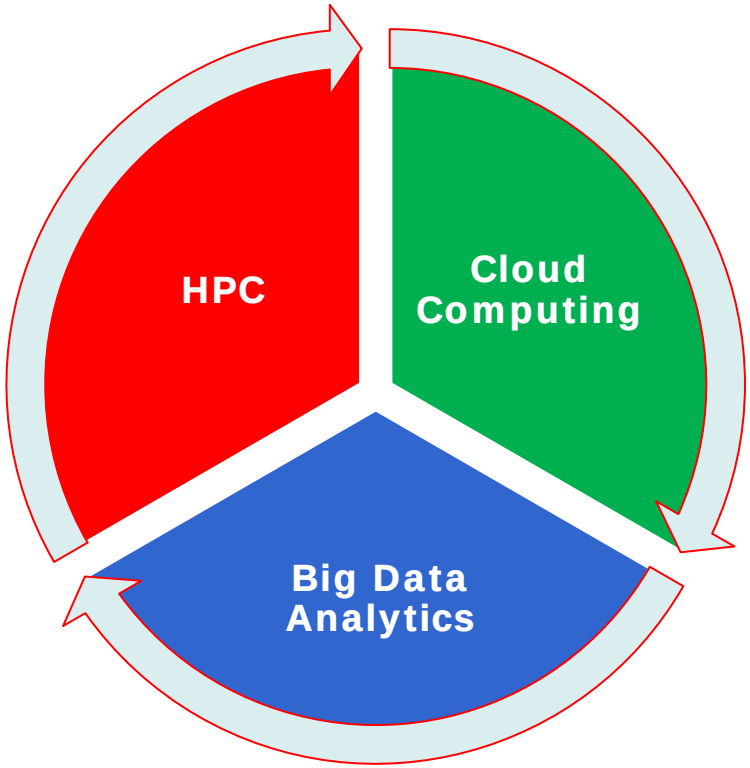
Head of Unit – High Performance Computing & Quantum Technologies
DG CONNECT, European Commission

HPC/EDI Objectives

- **Acquisition** (in 2020-2021) of 2 operational **pre-exascale** and (in 2022-2023) two full **exascale** machines (of which one based on European technology)
- **Interconnection and federation** of national and European HPC resources and creation of an HPC and Big Data service infrastructure facility
- **Demonstrating and testing** technology performance towards exascale through scientific & industrial compute-intensive applications

Aim: Build a world-class European High Performance Computing (HPC), Big Data (BDA) and Cloud Ecosystem

Enabled by the Convergence of 3 big technologies



- Major investments so far both at MS and EU level [FP7, H2020]
- Numerous research players (academia and industry)
- HPC and Big Data PPPs, PRACE, GEANT, etc.

HPC/EDI: EU investments

FET & LEIT Calls: technology development, integration, pilot test-beds and applications

- ➔ Technology development (low-power processor, SW, applications)
- ➔ Integrating and co-designing extreme scale systems

HPC – Cloud – BDA Ecosystem development

Two pre-exascale

Two exascale

Infrastructure/CEF calls

- ➔ Centres of Excellence, Ecosystem development
- ➔ Procurement and services for EDI/HPC infrastructures (exascale, big data nodes, interconnection) and use widening

HPC/EDI in Horizon 2020 Work Programmes

2014-2015	2016-2017	2018-2020

LEIT ICT WP ➔ Microprocessor, integration & demonstration

- Low-power processor design and development
- Co-design of extreme scale demonstrators
- HPC/BD/Cloud: Large scale testbeds and applications using existing HPC

FET WP ➔ Key components & concepts: preparing next generation & thereafter

- Components: Towards pre-exascale
- system architectures
- SW
- extreme scale, power-efficient and resilient HPC compute & data technologies and prototypes for (post-) exascale application performance
- Co-design of extreme scale HPC systems and demonstrators

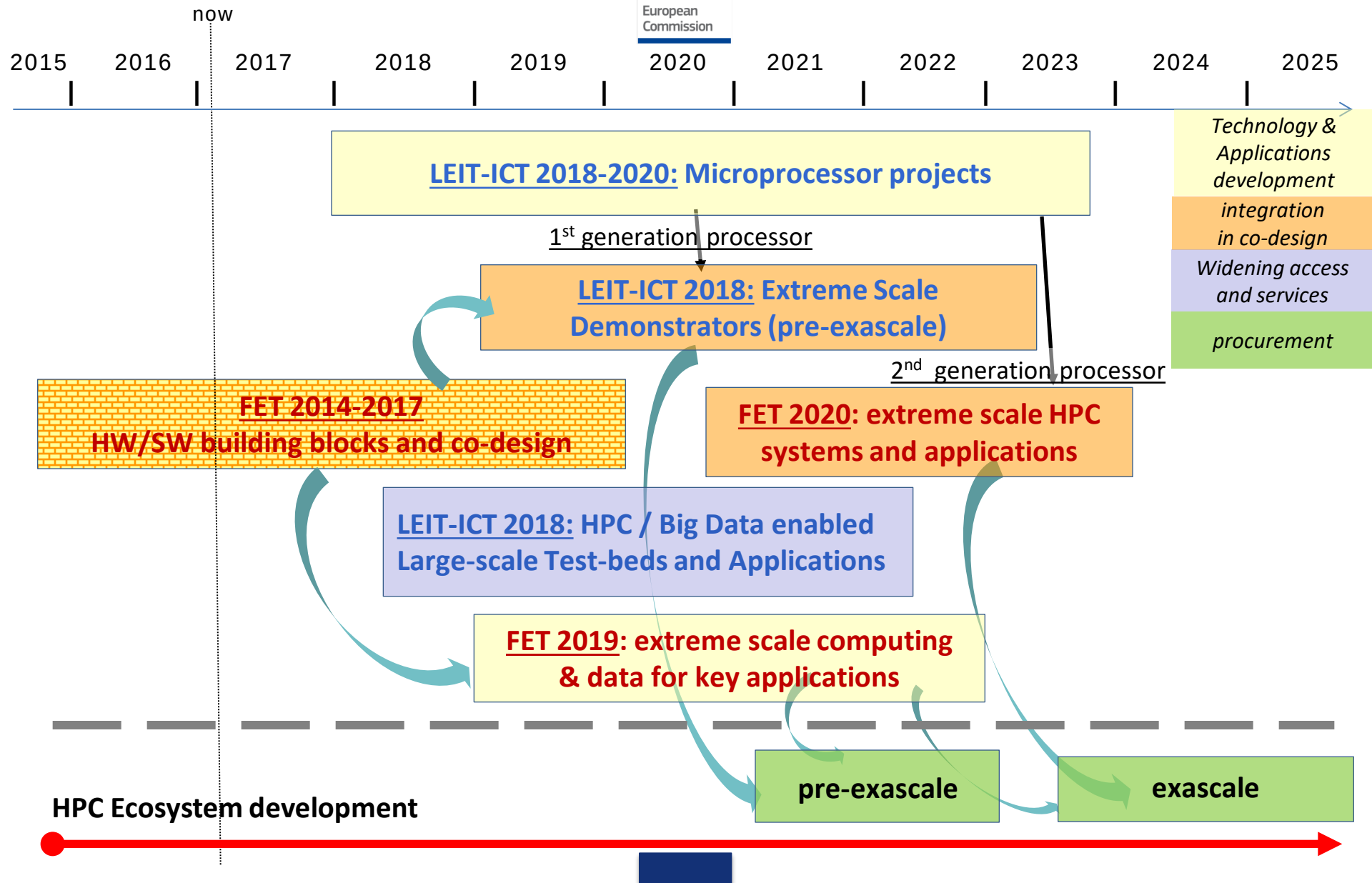
eINFRA WP and Connecting Europe Facility (CEF): Infra support & Procurement

- widening HPC-enabled BD services for stakeholders
- PRACE, GÉANT, Centres of Excellence
- Pre-exascale systems,
- Data nodes, Interconnectivity

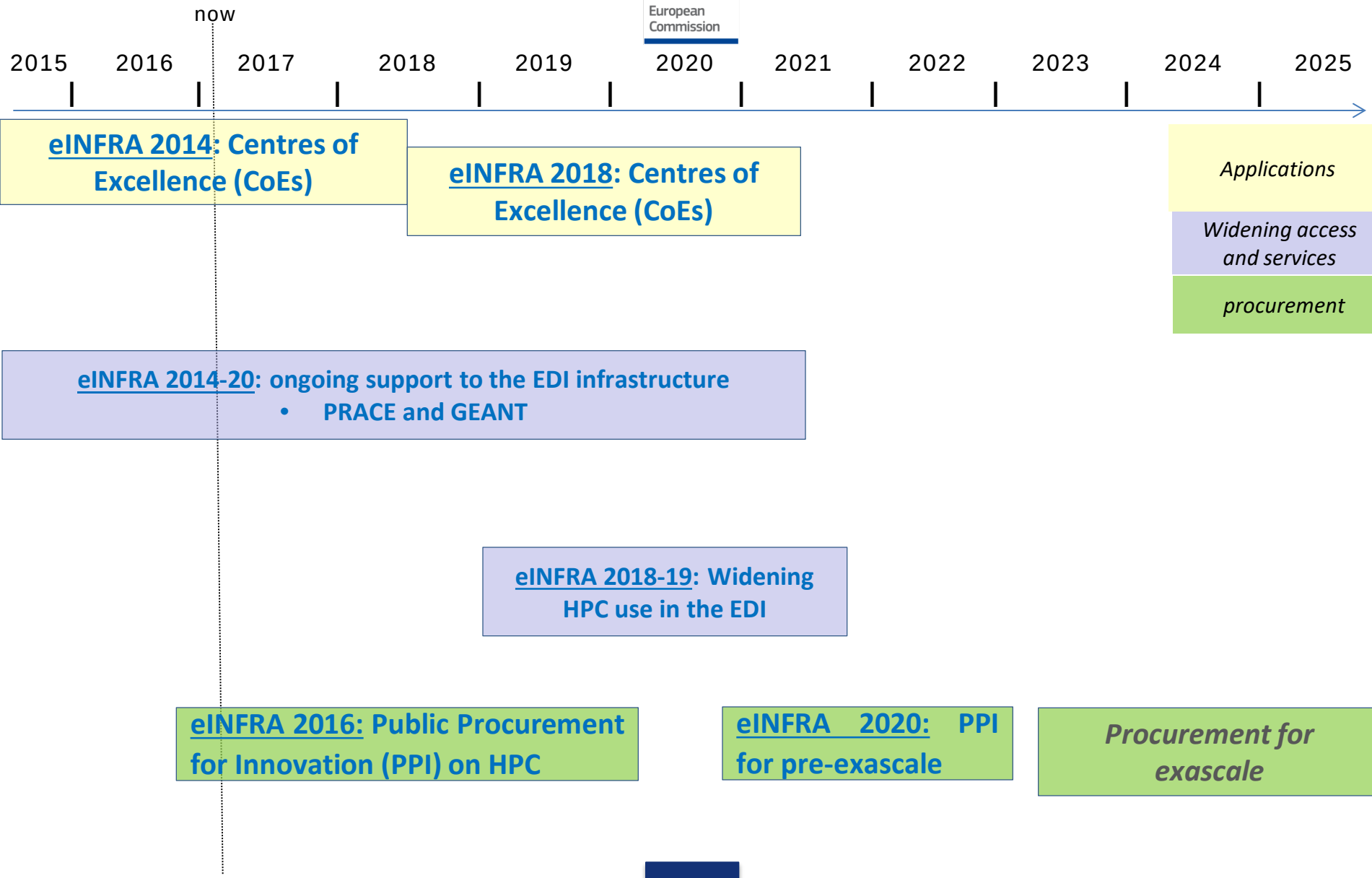
HPC timeline LEIT/FET (indicative)

European Commission

subject to discussion with committees



HPC timeline eINFRA (indicative)



Conclusions

An articulated implementation to realise the political ambition

- *Clear roadmap and timeline*
- *Coordinated actions using all mechanisms of H2020*
- *Creating and covering the full HPC ecosystem*
  - Technology development
  - Co-design and integration
  - Applications and test-beds
  - HPC infrastructure development
  - Widening use of HPC
- *Further strong cooperation with MS*
- *Governance structure on HPC/EDI (Rome 23/03)*

THANK YOU!

DISCUSSION