Welcome!

European Exascale Processor & Memory Node Design

www.exanode.eu

ExaNoDe Contrubutions to Extreme-Scale Demonstrators

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CEA

18th May 2017, 2-7pm, Barcelona, Catalunya @ European HPC Summit Week
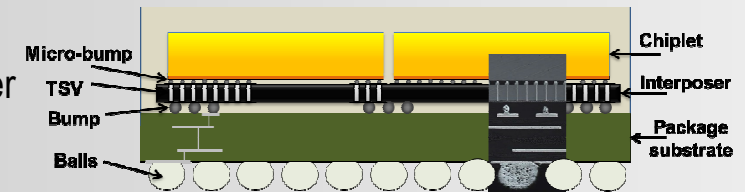
ExaNoDe Project

ExaNoDe is about compute node aiming:

- Energy Efficiency.
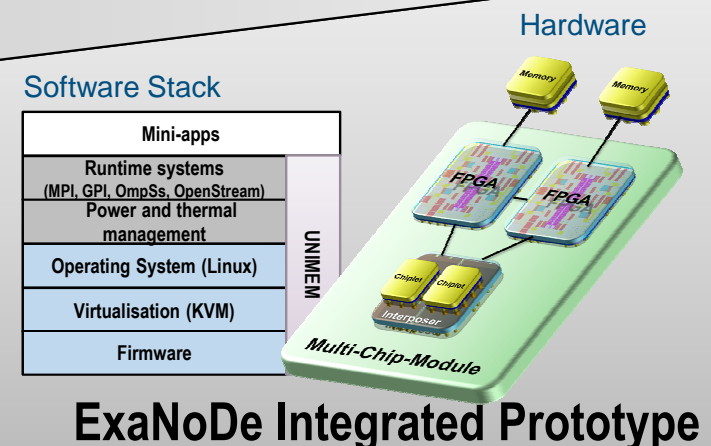- Dense Integration.
- Affordability.

ExaNoDe Core Technologies for compute node:

- System architecture:
  - ARMv8, GAS and coherent island
- Silicon Integration:
  - 3D integration/chiplet/interposer
  - Multi-chip-Module
- Software stack:
  - FW, OS, Virtualization, Programming models, Runtimes, Mini-apps

ExaNoDe objectives:

- **To deliver a compute element** integrating core technologies consistent with HPC system sizings and requirements for exascale computing.
- **To validate core technologies** applicability across a relevant set of HPC application domains.

Software Stack

Hardware

| Mini-apps |
| Runtime systems (MPI, GPI, OmpSs, OpenStream) |
| Power and thermal management |
| Operating System (Linux) |
| Virtualisation (KVM) |
| Firmware |

UNIMEM

ExaNoDe Integrated Prototype

ExaNoDe eco-system:

System archi.	Acceleration with FPGA	Compute node	Interconnect, storage & cooling
EURO SERVER	ECOSCALE	ExaNoDe	ExaNeSt
FP7		FETHPC-2014	EuroEXA FETHPC-2016
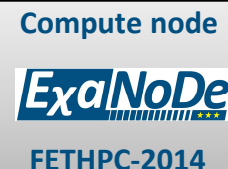
Suggested technologies for inclusion in an EsD
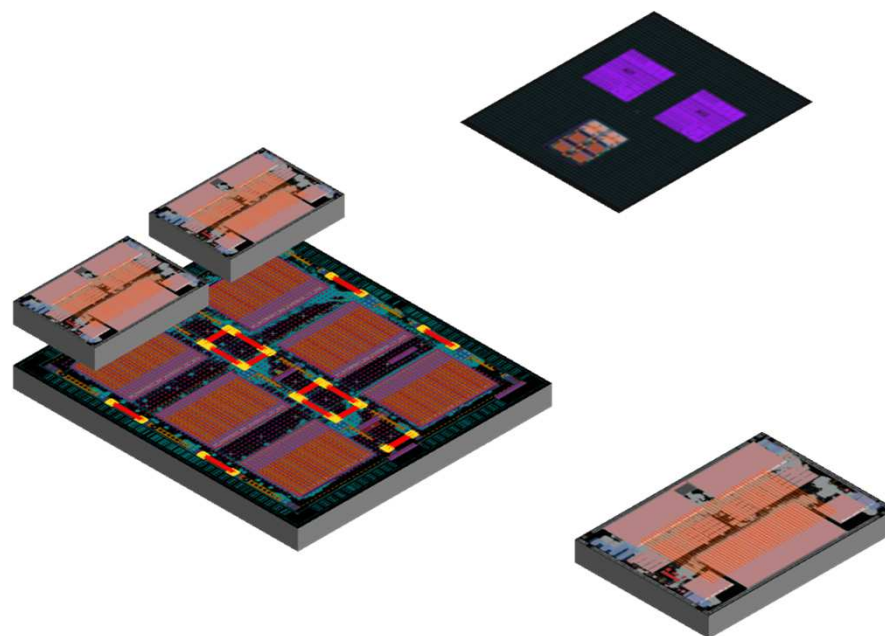
ExaNoDe prototype

Test Bed

SW stack

Board

Multi-Chip-Module

Interposer & 3D Integrated Circuit

System-on-Chip

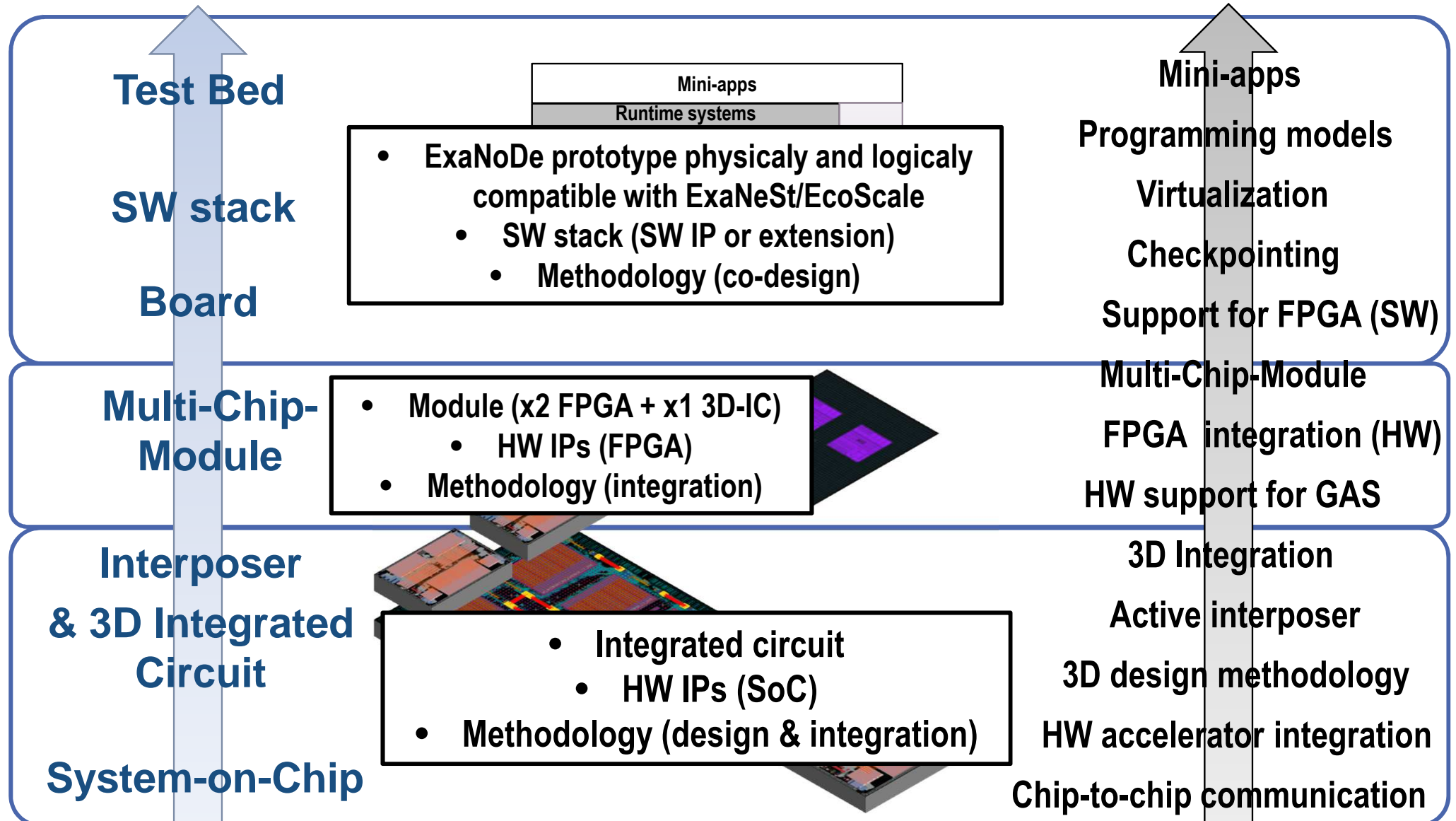| Mini-apps	
Runtime systems (MPI, GPI, OmpSs, OpenStream)	UNIMEM
Power and thermal management	
Operating System (Linux)	
Virtualisation (KVM)	
Firmware	

ExaNoDe technologies

Mini-apps

Programming models

Virtualization

Checkpointing

Support for FPGA (SW)

Multi-Chip-Module

FPGA integration (HW)

HW support for GAS

3D Integration

Active interposer

3D design methodology

HW accelerator integration

Chip-to-chip communication

ExaNoDe

ExaNoDe technologies: type

ExaNoDe prototype

ExaNoDe technologies

Test Bed

SW stack

Board

Mini-apps

Runtime systems

- ExaNoDe prototype physicaly and logicaly compatible with ExaNeSt/EcoScale
  - SW stack (SW IP or extension)
    - Methodology (co-design)

Mini-apps

Programming models

Virtualization

Checkpointing

Support for FPGA (SW)

Multi-Chip-Module

- Module (x2 FPGA + x1 3D-IC)
  - HW IPs (FPGA)
- Methodology (integration)

Multi-Chip-Module

FPGA integration (HW)

HW support for GAS

Interposer & 3D Integrated Circuit

System-on-Chip

- Integrated circuit
  - HW IPs (SoC)
- Methodology (design & integration)

3D Integration

Active interposer

3D design methodology

HW accelerator integration

Chip-to-chip communication

ExaNoDe technologies: maturity and reusability

- **Maturity:**
  - all technologies will be integrated and validated into the ExaNoDe prototype.

- **Reusability:**
  - Technologies are developed to be as generic as possible, but extra work for adaptation into specific project requirements may be required.

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