



EUROPEAN TECHNOLOGY
PLATFORM FOR HIGH
PERFORMANCE COMPUTING

A large, abstract graphic in the background consisting of numerous thin, radiating lines and small dots in various colors (white, yellow, orange, blue) against a teal background, creating a sense of dynamic movement and data flow.

ANNUAL REPORT 2018

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@etp4h

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ANNUAL REPORT 2018



Editorial

JEAN-PIERRE PANZIERA,
ETP4HPC CHAIR

Dear ETP4HPC Members and Partners,

It may be a fact known to only a few of you but I am an avid mountaineer. I am one of a team of old friends and each year we try to do at least one challenging Alpine route – ‘challenging’ according to our abilities, with some of us finding ‘the challenge’ part of it more demanding with the passing of time. When you scale a mountain such as Dôme de Neige des Écrins or Pic Coolidge, the most beautiful moment is not when you reach the summit – the most poignant moment is when you realise that the summit is within your reach, that you’re going to make it to the top, sound and in one piece. It usually happens when you pass the crux, the most difficult part, and you still feel strong enough to keep going and have the end of the journey in full view.

If you are part of the European HPC ecosystem, you should consider yourself very lucky, because we are past that inflexion point. The efforts made since the beginning of our journey, i.e. since the establishment of ETP4HPC and the beginnings of the construction of the European HPC eco-system, are paying off. We have a vibrant ecosystem in place meeting the needs of all users and we have over 150 technology project results to build on. Our instinct was right when we began working with BDVA – we are now working with our Big Data counterparts on the main advisory body of EuroHPC and we are extending this collaborating pattern onto other areas: the Internet of

Things and Artificial Intelligence. The EXDCI2 project constitutes an excellent mechanism to develop those collaborations.

As we speak, we are finishing our Vision document and we are embarking on the preparation of our next Strategic Research Agenda (SRA). This SRA will be the source of priorities for the research projects driven by EuroHPC. I encourage you all to take part in the writing of the SRA. We will need to work very closely with all stakeholders and projects, in particular with the European Processor Initiative, in order to deliver a vision that will allow EuroHPC to reach its main objective: independent access to HPC resources for European users.

We also need to think about the way back from the summit – to use another mountaineering analogy. We should focus on the areas where Europe can achieve long-term leadership. I encourage our members to reflect on the new challenges emerging from the discussions associated with the SRA, e.g. end-to-end computing, complex workflows, etc.

The rest of our journey will take place in close cooperation with EuroHPC, and we should focus on ensuring that we combine efforts for the best benefit of the European HPC value chain and its stakeholders. Please participate actively in this complex process as such a chance will not happen again. This is the time to make it happen, to shape the future of European HPC. Thank you for all your support to date. ■

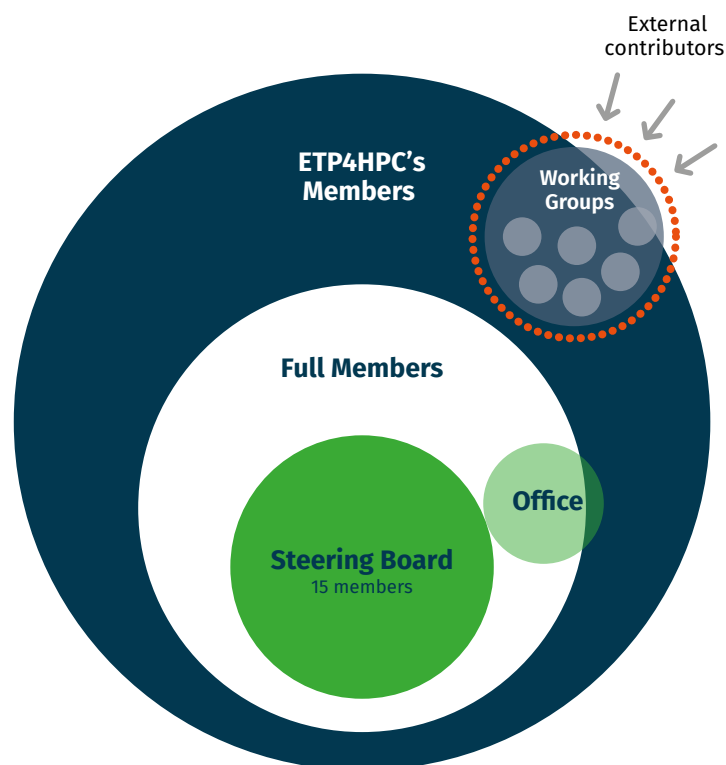
Our association

ETP4HPC, the European Technology Platform in the area of High-Performance Computing (HPC), was incorporated as a Dutch association in June 2012. We are an industry-led think tank gathering European HPC technology stakeholders: technology vendors, ISVs, service providers, research centres, and end users.

Our main objective is to increase the global market share of the European HPC technology vendors. Our main deliverable is our Strategic Research Agenda (SRA) which defines the priorities of the European HPC technology research programme managed by the European Commission.

Until 2018, the ETP4HPC association represented the European HPC industry in the dialogue with the European Commission within the HPC contractual Public-Private Partnership (cPPP). As of 2019, the role of the HPC cPPP is taken over by the EuroHPC Joint Undertaking (JU), in particular regarding HPC R&I funding and steering. In this new context, ETP4HPC will continue to help shape Europe's HPC Research Programme. ETP4HPC is a private member of the EuroHPC JU, and well represented in its Research and Innovation Advisory Group.

OUR ORGANISATION



The ETP4HPC Steering board



The current Steering Board was elected at the Annual General Assembly on 13 March 2018, for 2 years. Its current members represent:

- **European Research centres** (5 seats):
BSC, CEA, Cineca, Fraunhofer, Forschungszentrum Jülich
- **European SMEs** (4 seats):
E4 Computer Engineering, ParTec, Megware, Clustervision
- **European-controlled corporations** (4 seats):
Atos, ESI Group, Infineon, Seagate
- **International companies with R&D in Europe** (2 seats):
Fujitsu, Intel

The Steering Board appointed the following Steering Committee:

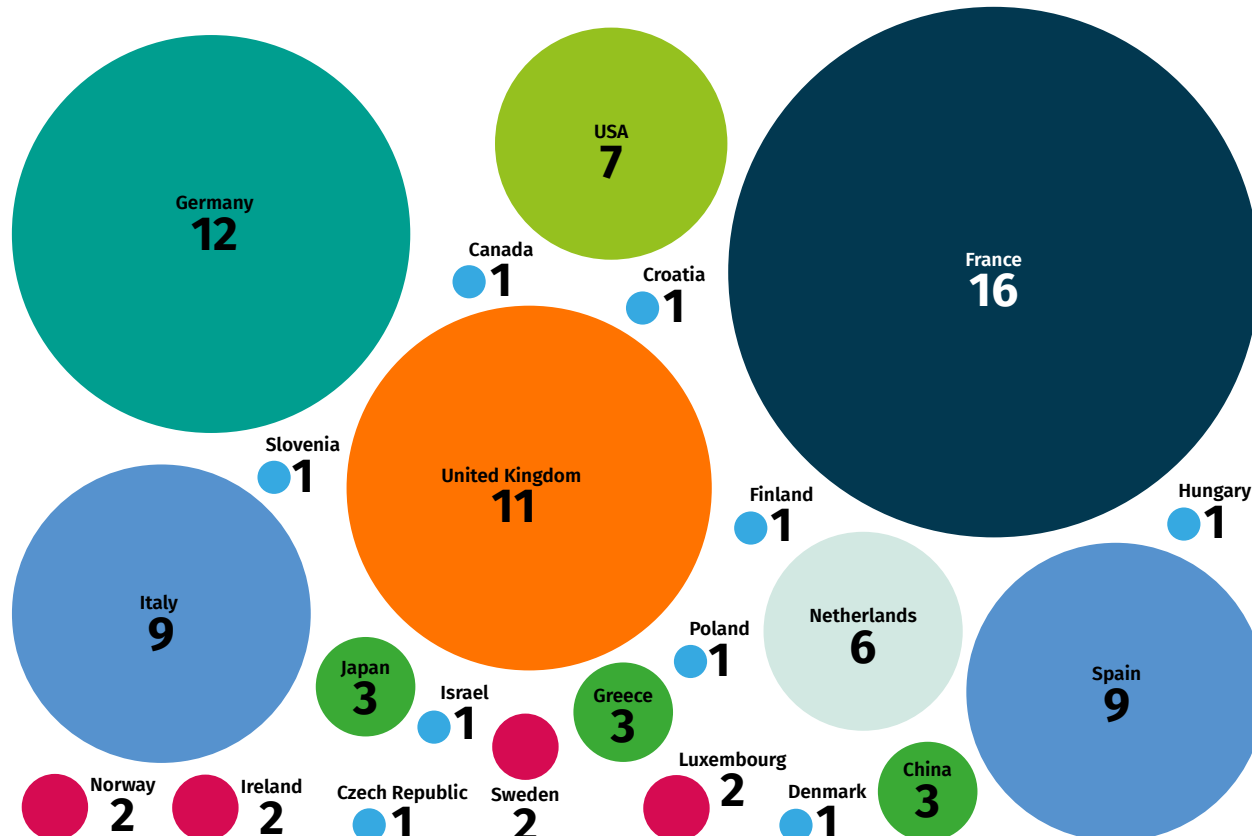
- **Chairman:**
Atos - Jean-Pierre Panziera
- **Vice-chair for Research:**
CEA - Jean Gonnord
- **Vice-chair for Industry:**
Seagate - Sai Narasimhamurthy
- **Secretary:**
ParTec - Hugo Falter
- **Treasurer:**
ClusterVision - Frank van der Hout

Office

ETP4HPC has a distributed Office team, based in France, Spain, Germany and the Netherlands. The Office is in charge of day-to-day operations, under the supervision of the Steering Board.

- Pascale Bernier-Bruna (Atos) is our communication leader and community manager
- Carolien Deklerk (Clustervision) is our accountant, covering all financial aspects
- Ina Schmitz (Partec) is in charge of logistics related to the Steering Board meetings. Since January 2019, Chris Ebell (Partec) has taken over this role
- Maïke Gilliot (Teratec) manages ETP4HPC's contributions to the H2020 funded support actions EXDCI-2 and HPC-GIG and contributes to out-bound activities, such as workshops
- Michael Malms (IBM) is leading our SRA efforts
- Jean-Philippe Nominé (CEA), coordinates the Office team and supports the Chairman
- Marcin Ostasz (BSC) co-manages our road-mapping effort and industrial relations

OUR 96 MEMBERS REPRESENT 23 COUNTRIES



BREAKDOWN OF OUR MEMBERS BY STATUTE AND PROFILE

Our membership grew by 12% over the last year, with the majority of new members coming from the private sector.

STATUTE

58 Full members

10 SMEs

15 Industrial organisations

33 Research organisations

38 Associated members

26 SMEs

3 Industrial organisations

6 Research organisations

3 Associations or individuals

PROFILE

54 Private sector

36 SMEs

18 Industrial organisations

42 Public sector

39 Research organisations

3 Associations or individuals

News from our Working Groups

WORKING GROUP ON TECHNOLOGICAL ROAD MAPPING:

This Working Group continued in 2018 the main activity of the association - the elaboration of research priorities and related recommendations - by providing input to the HPC-related Work Programme 2019 and 2020 and by preparing our HPC Vision for the new 2021-2027 EC research programme ("Horizon Europe", the 9th Framework Programme).

The Working group organised many workshops throughout the year to develop our recommendations, jointly with our members and external experts from BDVA, HiPEAC and AIOTI.

Contact: Michael Malms

ENERGY EFFICIENCY WORKING GROUP

The Working Group on Energy Efficiency organised a half day workshop during the European HPC Summit Week in Ljubljana, tackling the energy efficiency problem from different perspectives: covering hardware aspects as well as software-based solutions. For 2019, a similar workshop is planned within ISC.

Contact: Michael Ott

INDUSTRIAL USER WORKING GROUP

The Industrial User Working Group is actively seeking to engage more HPC Users in ETP4HPC, focusing at this stage on large companies with solid experience in HPC usage. The group is engaging with some key users in order to understand their needs and to validate ETP4HPC's approach.

Contact: Ingolf Stärk

EuroHPC: leveraging the assets of European HPC technology?

Gustav Kalbe, Head of the High Performance Computing and Quantum Technologies Unit of the European Commission and also the Interim Executive Director of the EuroHPC Joint Undertaking .

The EuroHPC Joint Undertaking (JU) brings together the EU (represented by the European Commission), 25 EU Member States and countries associated to Horizon 2020 that have decided to join, and private members ETP4HPC and BDVA.

The Euro HPC JU is a legal and funding entity which enables the pooling of EU and national resources in High-Performance Computing.

More information:

<https://eurohpc-ju.europa.eu>

EuroHPC on Twitter: @EuroHPC_JU



It is a pleasure to address the members of the ETP4HPC Association. You have closed another successful year while our ecosystem passes over the inflection point of its growth. Your organisation has played an extremely important role in the building of Europe's HPC ecosystem. Looking back a decade, Europe's activities in the area of HPC were not fully coordinated. We did not have an entity representing our HPC technology providers, we had a limited number of technology projects in place and our application expertise was not organised in the highly successful Centres of Excellence. Your association has been instrumental not only in helping us, the European Commission and the European politicians, understand the needs of the European HPC technology industry and the optimal path for its rapid development, but also in motivating the rest of the ecosystem, in particular our application expertise and SME technology providers.

For the last few years, we have been working together within the contractual Public-Private Partnership, which has proven to be an efficient forum for exchanging updates and executing commitments. The results of this work are tangible – the impressive outputs of the first FETHPC projects and the potential of the on-going ones, including the co-design initiatives. Your input – the ETP4HPC Strategic Research Agenda and related documents – have served us well, in both preparing the calls and assessing the projects. I expect the Association not only to continue this work, but also extend your support as a Private Member of the EuroHPC Joint Undertaking.

Now, Europe is changing gear. I look forward to work very closely with your representatives within the EuroHPC Research and Innovation Advisory Board. Let us have a look at how it is going to benefit from the provision of European technology, a question dear to the hearts to many a member of ETP4HPC.

EuroHPC will continue the work of the previous programmes in the area of HPC technology research, but its main mission is different: to develop European technologies for the coming exascale era. EuroHPC combines funding from the European Union with funding from European states participating in the EuroHPC initiative. We want to deliver a European HPC infrastructure that is competitive with the best in the world. The first step is acquiring next-generation supercomputers and putting them into service for user applications by 2020. Then, we will aim to support research and innovation activities to deploy exascale machines in 2022 so users can continue to benefit from world-leading HPC technologies. Our infrastructure should primarily serve the European scientists, but there is a lot of interest among European companies in the application of European HPC technology. These certainly include car manufacturers and other large engineering companies, along with oil and gas firms, logistics companies, pharmaceutical, aerospace and IT companies.

We have two important assets: Europe has world-class strengths in applications and other HPC software. We also have centres-of-excellence to ensure users always have access to the best-available applications. Another European strength is our strong focus on co-design, on ensuring that HPC hardware and software are developed together with application performance in mind.

Our main challenge in Europe today is that we do not produce some key technologies for HPC, including microprocessors. We should be able to produce globally competitive European HPC systems that are based on indigenous European technologies and components. Being able to produce them ourselves is critical for Europe's strategic independence in HPC and for advancing applications.

We have a number of initiatives in Europe to develop missing technologies and we will see whether they are competitive in time for the procurements of the supercomputers the EuroHPC Joint Undertaking plans to acquire jointly with the EuroHPC Participating States. With an extreme-scale demonstrator machine, we intend to test whether the design for the European processor is stable, for example. The European Processor Initiative has established ambitious goals to achieve by 2025, including the development of an indigenous HPC processor, an embedded processor for automated vehicles and other AI applications, and an accelerator based on the RISC-V standard.

Our hope is that, by 2022, European technology will be mature enough to be globally competitive. However, European competitors will need to compete strictly on merit, although ideally we would like companies based in the EU to be able to develop the machines. However, we do not exclude per se a cooperation with non-EU vendors if that can satisfy our overall ambition of deploying competitive HPC supercomputers and ensure unrestricted access to strategic technology components.

Our expectations is that the European HPC ecosystem will keep growing at a cruising speed for the next years. Our vision is long-term. In 2025, we should have a fully interconnected infrastructure across Europe in HPC, connecting national and European machines. The fully meshed network will be available to any user in Europe, with a single point of entry where the user sends a request and it goes to the most appropriate machine and this process is completely transparent to the user. The user will not need to care where the application runs, whether it is on a national or European machine. The second expectation is that we manage to keep European science and industry competitive because they have had access to world-class HPC resources.

I wish you all the best in your endeavours. I look forward to see the technology developed by your teams push European HPC towards global leadership. ■

CoolIT**SME/ASSOCIATED MEMBER**

CoolIT specializes in scalable liquid cooling solutions for the world's most demanding data centres. Through its modular, rack-based Direct Liquid Cooling technology, Rack DCLC™, CoolIT enables dramatic increases in rack densities, component performance and power efficiencies.

From Passive Coldplate Loops specifically designed for the latest high TDP processors from Intel, NVIDIA and AMD, through to Coolant Distribution Units, CoolIT's reliable technology installs into any server or rack, ensuring ease of adoption and maintenance.

<https://www.coolitsystems.com/>

Constellcom Ltd**SME/ASSOCIATED MEMBER**

Constellcom's mission is to provide easy, secure and private access to on-premises HPC resources to anyone regardless of size and skills and for any application from its web-accessible Constellation™ platform. Constellation™ empowers HPC Centres and users by providing a collaborative environment to manage and access supercomputing resources when and where they are needed.

Constellcom was founded after our founding team had experienced first-hand the barriers to investigation that a shortfall in compute power can mean to any ground-breaking research. As users of HPC ourselves, we understand deeply the impact of hassle-free and self-managed access to HPC, strong collaboration amongst multi-skilled teams, and what that can mean for discovery and in turn, economics. Empowering engineers, scientists and innovators to run projects and remain in control of HPC is at the heart of Constellation™. As close collaborators to HPC Centres, we also understand the challenges of managing clients, allocations, accounts and systems. For HPC Centres, licensing Constellation™ means freedom and visibility both to manage internal resource and to optimise usage for external clients. Our team of expert scientists and engineers provide assistance to HPC Centres with their management and support industrial users with software acceleration and adaptation to HPC, simulations and workflows.

<https://www.constellcom.com/>

Infineon**Inspur****EUROPEAN CORPORATION/FULL MEMBER**

Infineon Technologies AG is a world leader in semiconductor solutions that make life easier, safer and greener. Microelectronics from Infineon is the key to a better future.

In the 2018 fiscal year (ending 30 September), the Company reported sales of around €7.6 billion with about 40,100 employees worldwide. Infineon is listed on the Frankfurt Stock Exchange (ticker symbol: IFX) and in the USA on the over-the-counter market OTCQX International Premier (ticker symbol: IFNNY).

<https://www.infineon.com/>

GLOBAL CORPORATION/ASSOCIATED MEMBER

Inspur is a global leader in computing technology innovation. It's renowned for building customized platforms that converge HPC, AI, and cloud computing. Gartner has ranked Inspur as China's largest server manufacturer and among the Top 3 in the world. With a focus on innovation, Inspur has proven capabilities in HPC system research, design & deployment, after-sale service, operations, and maintenance of more than 17% HPC systems in of TOP500 list, which ranks Inspur as No. 2 global manufacturer for the total number of systems in the TOP500 supercomputers. Inspur offers complete HPC hardware & software product lines and application development services.

Inspur has accrued extensive experience in complete Petascale HPC system designs including the development of many cutting edge HPC applications. Inspur HPC has helped many business and organizations achieve, for their first-time, precise calculation results that simulate untestable real-world scenarios to predict complex future outcomes. These solutions have been used to: make people's lives healthier with the use of precision medicine for early diagnosis; model and predict large scale catastrophes/natural disasters; and helped large companies and SMEs to manufacture intelligently to deliver world-class products and services. Inspur has pushed the innovation envelope by converging HPC with other cutting-edge disciplines like AI and machine learning to solve a myriad of critical business challenges for its clients – a fact that steers Inspur ahead of several renowned industry peers.

Inspur is devoted to providing the European HPC community with extreme HPC hardware design and heterogeneous acceleration technologies for Parallel Computing, Big Data, Cloud Services, Artificial Intelligence, etc. As a complete and end-to-end HPC solution provider, Inspur specializes in providing "turnkey projects" to customers from underlying HPC hardware infrastructure, cluster management system and software stack, HPC application development, and performance tuning services.

<http://en.inspur.com/>

LINKS Foundation



RESEARCH ORGANISATION/FULL MEMBER

The LINKS Foundation was founded in 2016, exploiting and enhancing the experience gained - from the Istituto Superiore Mario Boella (ISMB) and from the Istituto Superiore on Territorial Systems for Innovation (SiTI) - in the field of research applied and technology transfer, adding a fundamental element such as the enhancement of the research result. As part of the knowledge chain, the Foundation intends to enhance the lever of applied research, contributing to the growth of the socio-economic system by relating the academic world, the public and private sectors, activating large-scale processes and projects with significant impacts on territory. The Foundation is an ideal partner for both SMEs, which can enhance the ability to develop innovation and gain competitiveness using the experience and expertise of the foundation, both of the large enterprises that can, in partnership with it, develop new ideas and new technologies. The Foundation today relies on the technological and process competences of around 150 researchers working in close cooperation with companies, academia and public administration. LINKS is organized in research areas focused on some core sectors of ICT. Within the field of HPC systems, LINKS is active in the following two main topics.

- 1) Applied research in Advanced Computing with: the study and design of distributed computing architectures based on public and private cloud platforms; low power architectures in high performance perspective; orchestration of heterogeneous architectures in computing continuum; resources and applications management in distributed environment; application analysis, design and development for machine learning, HPC-embedded context through many-core architecture.
- 2) Applied research in Data Science for extreme scale analysis of Big Data, including: the design of distributed databases and processing architectures for heterogeneous types of data; the development of distributed Data Mining and Machine Learning algorithms for different applications.

<https://linksfoundation.com/>

Mellanox



GLOBAL CORPORATION/FULL MEMBER

Mellanox Technologies is leading supplier of end-to-end Ethernet and InfiniBand intelligent interconnect solutions and services for servers, storage, and hyper-converged infrastructure.

Mellanox intelligent interconnect solutions increase data centre efficiency by providing the highest throughput and lowest latency, delivering data faster to applications and unlocking system performance. Mellanox offers a choice of high performance solutions: network and multicore processors, network adapters, switches, cables, software and silicon, that accelerate application runtime and maximize business results for a wide range of markets including high performance computing, enterprise data centres, Web 2.0, cloud, storage, network security, telecom and financial services.

<http://www.mellanox.com/>

Neovia



SME/ASSOCIATED MEMBER

NEOVIA Innovation is an SME service company based in Paris and Lyon, France.

NEOVIA Innovation supports the development of innovative structures – either private or public – and their ecosystems. From the conception to market implementation, NEOVIA Innovation offers services covering all the phases of complex collaborative projects. The company has a long record of acting as a Project Management Office, working side by side with the project coordinator to bring support to the partnership, with a strong experience in EU-funded projects.

NEOVIA Innovation has a specific knowledge on Applied Mathematics, Numerical Analysis and High Performance Computing, Big Data and Extreme Computing. The company has been involved for years in the European High Performance Computing Ecosystem, notably through its participation in past and present European HPC initiatives such as EESI, EESI-2, EXDCI and EXDCI-2. NEOVIA Innovation regularly takes part in the BDEC international initiative.

<https://www.linkedin.com/company/neovia-innovation/>

Saiver SRL



SME/ASSOCIATED MEMBER

Saiver designs and manufactures a multi-purpose, highly energy efficient, custom and “self-contained” Prefabricated Modular Data Center solution (MDC). The Saiver solution is the perfect choice for universities, research centers, private companies or government organizations that are facing the need to build micro, small or large HPC facilities but have budget and timing constraints. Saiver was founded in 1959 in Monza (Italy) and has been designing and manufacturing high quality, custom Air Handling Units, for more than half of a century now. Saiver Series A1 AHUs are delivered in more than 44 countries in the world, making Saiver to be recognized as a technology and quality leader. Further confirmation of the full commitment to quality is the fact that 100% of Saiver AHUs are Eurovent certified. Thanks to its long experience in precision air treatment, adiabatic cooling, modular structures and insulated sandwich panels, more than 10 years ago Saiver has developed an innovative, flexible, and “self-contained” Prefabricated MDC solution with unparalleled energy and water saving performances in any climatic zone. Important research centers, around the world, have selected the Saiver MDC solution to host their HPC equipment, instead of building rigid, inefficient and expensive “brick and mortar” facilities. Among the customers that are running their Supercomputers into a Saiver MDC we can mention:

- NASA AMES Research Center (USA)
- LLNL (USA)
- NETL (USA)
- CSC (Finland)
- CCFE (UK)
- Observatoire de Paris (France)

“Efficiency by Design”: as witnessed by Saiver HPC customers, the naturally “chiller free” Saiver MDC solution, each year saves them millions of kW/h thanks to its very low mechanical PUE (down to 1.02), as well as millions of potentially wasted liters of water. Moreover, Saiver MDC dramatically reduces the CapEx, the time, and the space needed for the construction of the HPC facility, compared with the traditional “brick and mortar” approach.

<http://www.saiver.com/en/home/>

Submer



TS-JFL



SME/FULL MEMBER

Submer, the Cleantech company, designs, manufactures and installs the SmartPods, a liquid Immersion Cooling solution for any IT infrastructure, hardware and application: HPC, Hyperscalers, Data Centers, Edge, AI, Deep Learning, blockchain, etc. The SmartPods are the most practical, resilient, and highly efficient Immersion Cooling solution that stand out for:

- Modular, compact design.
- Being an all-in-one solution.
- Using a dielectric fluid (SmartCoolant) with a long lifecycle, completely biodegradable and non-hazardous for people and environment.
- Saving between 95% and 99% of cooling costs (representing 50% of the electricity bill).
- Saving 85% of physical space.
- Guaranteeing a PUE <1.03 anywhere in the world.
- Achieving unprecedented IT Hardware densities in a limited space (>100kW per rack footprint).
- Reducing building cost.
- Increasing deployment speed with Edge ready solutions.

Submer was founded in 2015 by Daniel Pope and Pol Valls to make operating and constructing Data Centers more sustainable. Both Daniel and Pol have previous track records of taking tech ventures from startups to high-value companies (notably, creating, growing and operating the Data Center Datahouse Internet, later acquired by Telefónica Group in 2011).

With offices, R&D lab and manufacturing plant located in Barcelona, the multi-disciplined world class team brings together skills and experience in Data Center operations, thermodynamics engineering, HW & SW development, service delivery and innovation management, working with leading companies around the globe.

<https://submer.com/>

SME/ASSOCIATED MEMBER

Technology Strategy is a consulting company. Its main competence is to analyse the potential of new IT technologies (how they can be successful in the IT market) and the impacts of IT innovations on the strategy of large companies and SMEs.

Technology Strategy is a third party in the EXDCI-2 coordination action. It currently works on the analysis of

- new nanoelectronics or photonics technologies relevant for the future of HPC,
- the current landscape of HPC research projects,
- the international development of HPC.

<http://www.ts-jfl.net/>

UCit



University of A Coruña



SME/ASSOCIATED MEMBER

UCit* is a new kind of HPC Solution Provider.

At UCit we do focus on usage rather than technology itself. We firmly believe that scientists, engineers, analysts should not spend their time trying to understand how infrastructure works nor trying to fix it.

We know that more than ever, they need to collaborate – share and access data across HPC resources which are distributed across organisations and geographies.

We understand that flexibility and ease-of-use is critical to support their evolving requirements from Machine Learning and Decision Making to traditional HPC workloads.

We acknowledge that Computer Science is a Science and Exascale (or more...) is a critical resource needed to support the most important challenge humanity is facing. Simultaneously, at a smaller scale we will continue to act to democratize HPC through a true move towards HPC-as-a-Service.

UCit helps public and private organisations of all sizes to access and use seamlessly HPC resources on-premises, on HPC Centers or on public clouds.

- We develop data-analysis (Analyze-IT) and machine learning (Predict-IT) software tools to understand how to optimize on-premises HPC usage.
- We enable HPC-as-a-Service to integrate Batch and Interactive workloads and to secure access to data and applications.
- We understand which workload can effectively move to public cloud, at which cost through our WorkCloud methodology, we prototype and run it in production.

We work towards the development of an “HPC Wind Tunnel” to enable the creation of such services. Our approach is European and Collaborative. We look forward to future opportunities to work on projects together

*Pronounce “You See it!!!”

<https://www.ucit.fr/>

RESEARCH ORGANISATION/FULL MEMBER

The University of A Coruña (UDC) is a public institution whose primary objective is the generation, management and dissemination of culture and scientific, technological and professional knowledge through the development of research and teaching. The ICT Research Center CITIC is a singular research center of the University of A Coruña, whose main objective is to promote the advancement and excellence in research, development and innovation in Information and Communications Technologies (ICT) and to promote the transfer of knowledge and results to the society. The CITIC, with more than 250 researchers including senior, postdoctoral and pre-doctoral researchers, has its research activity organized around three main technology areas:

- Data and Information Science: Big data, machine learning, statistics, mathematical models and simulation, information retrieval, GIS, document management systems and web information, quantum computing.
- Perception, cognition and interaction: artificial intelligence, artificial vision, recommendatory systems and gamification, cybersecurity.
- Computer architecture, sensor and communications: High Performance Computing, Internet of Things, wireless communications, cloud computing, distributed systems.

With more than 30 University-Industry collaborative projects per year, CITIC is a meeting point between the UDC research groups and ICT companies of the Galicia region and Spain.

CITIC researchers have conducted a wide range of work on HPC topics such as developing parallel applications for different parallel architectures and programming paradigms (clusters, shared memory multiprocessors, GPUs), optimizing code exploiting underlying processor architecture, design of fault tolerant applications, cloud computing application deployment and massive data set processing. Multiple funded research projects have been developed around these topics at national and international level.

<https://www.citic.udc.es/>

FET-HPC 2015 projects: A Wealth of Results!

Jean-François Lavignon,
EXDC12

Most of the European FETHPC projects from the September 2015 call have now been completed. It is a good time to analyse their outcomes and identify recommendations for maximizing their impact.

First, let us have a look at the topics addressed by the 19 projects! The following classification reflects well the range of their topics:

HPC system focused projects

From package to system ExaNoDe - ExaNeSt - ECOSCALE

ARM based HPC Mont-Blanc

Reconfigurable systems EXTRA - MANGO - Green Flash

IO Sage - NEXTGenIO

HPC stack and application-oriented projects

Energy efficiency ANTAREX - READEX

Programming model INTERTWinE

Multiscale ComPat - AllScale

Generic applications: ExaHyPE - ExCAPE - ExaFLOW - NLAFET - ESCAPE
Hyperbolic PDE, Machine learning,
Fluid dynamics, Numerical linear algebra,
Weather models

All the projects have taken part in a dedicated survey (run by EXDC12) out of which a list of the most relevant outputs (i.e. 'IPs': intellectual property elements) generated by the projects has been produced. A simple quantitative analysis shows that most of the results are in the field of software. Out of the 171 IPs listed, 114 (two third) are software and 20 are hardware related.

The other types of results are APIs, applications optimizations, benchmark suites, trainings and demonstrators.

Interestingly, most of the IPs produced could be exploited. They address the needs of different types of users or stakeholders that can be represented in the following table:

	API	application optimisation	benchmark suite	demonstrator	HW	report	SW	training	Total
Application developer	7						39	4	50
Application developer/ computing centre				8			4	1	13
Application developer/ end user							10		10
Computing centre		1	4				5		10
End user		6				2	34	2	44
ESD					4		5		9
HPC system customer					1				1
HPC system provider					13		9		22
HPC system provider/ application developer					1		3		4
HPC system provider/ computing centre			2				4		6
HPC system provider/ Processor provider					1		1		2
TOTAL	7	7	6	8	20	2	114	7	171

It is clear that the FET HPC 2015 projects have generated a lot of IPs that can be useful for end users and application developers. Some of them target HPC system providers, computing centres or could provide valuable technologies for integration projects (such as ESDs, Extreme Scale Demonstrators).

Qualitatively, in the hardware area, one should note the development of several processor or FPGA boards, active interposer technology, interconnect technologies (one using photonics) and cooling technology.

The system-oriented projects have developed 8 demonstrators, most of them open to experiment by external teams. The larger ones in terms of computing power come from ExaNest/ EcoScale, Mont-Blanc and Mango. The IO-related projects, Sage and NextGenIO have also produced demonstrators that can be used for testing new storage hierarchy or object file system. Some APIs have been proposed by the projects in domains such as FPGA management, object file system, energy efficiency and interaction between runtimes.

In the software area, besides the enhancement of several applications or application kernels, there are results in domains such as FPGA programming, file systems, runtime, energy efficiency, time constrained computing, tuning/debugging tools...

The complete set of results is broad and diverse. The exploitation of this basis could be enabled by the new FET-HPC 2017 or other projects as they will continue some of the work (e.g. EuroExa, Montblanc2020, Sage2, Escape 2 or Recipe). In addition to these projects, it would be good to launch integration projects that could use and further develop some of the IPs generated. This vertical integration was one of the objectives of the ESD proposed by the HPC ecosystem. Based on the current results, we also suggest horizontal projects that will integrate some of the results that are closely related and complementary in one common framework. At least in domains such as FPGA programming, runtime and energy efficiency, it would be valuable to have open environments for the European HPC ecosystem.

To summarise, the FET-HPC 2015 call has produced an impressive set of IPs that could be reinforced by vertical or horizontal integration projects, thus pushing these new technologies toward industrialisation.

EXDCI, and now EXDCI 2 (European Extreme Data & Computing Initiative) supports the development and implementation of a common strategy for the European HPC ecosystem. PRACE and ETP4HPC are both involved in this transversal project.

More information:
<https://exdci.eu/>
EXDCI on Twitter: @exdci_eu



Targeted user Technology	ESD	HPC system provider	Computing centre	Application developer	End user
Computing node/ board	Ecoscale Exanode Mont-Blanc 3	Greenflash ExaNest Ecoscale Mont-Blanc 3 Exanode			
Interconnect Memory hierarchy	NextGenIO ExaNest Ecoscale	NextGenIO ExaNest			
Storage/file system	SAGE	SAGE	SAGE	ExaNest SAGE NextGenIO	
Tools for FPGA	MANGO EXTRA	MANGO Ecoscale		MANGO Ecoscale EXTRA	
Software stack	Greenflash EcoScale Antarex	MANGO Greenflash Mont-Blanc 3 Readex	MANGO NextGenIO Mont Blanc 3 COMPAT Readex Antarex	Readex Antarex	
Programming model/ tool	Exanode InterTwine	AllScale InterTwine	InterTwine	MANGO AllScale Greenflash MontBlanc3 Exanode InterTwine Antarex	ExaFlow
Optimization tools	Ecoscale			Greenflash Mont-Blanc 3 EXTRA Readex Antarex	NLAFET
Library				ExaFlow ExCAPE NLAFET Readex Antarex	NLAFET
Application		NextGenIO COMPAT Antarex	NextGenIO COMPAT Antarex		ExaNest ExaFlow ESCAPE ExHype ExCAPE NLAFET Readex Antarex

The technology stacks of High Performance Computing and Big Data Computing

What they can learn from each other

The paper this snapshot has been taken from, reflects an undertaking between two distinct ecosystems - the European associations for HPC (www.ETP4HPC.eu) and Big Data Value (www.BDVA.eu). This and other similar collaborations have been supported by the EXDCI and EXDCI2 projects.



Download the complete white paper

STACK OVERVIEW AND PROFILES

As some Big Data Computing (BDC) workloads are increasing in computational intensity (traditionally an HPC trait) and some High Performance Computing (HPC) workloads are stepping up data intensity (traditionally a BDC trait), there is a clear trend towards innovative approaches that will create significant value by adopting certain techniques of the other. This is akin to a form of “transfer learning” or “gene splicing” - where specific BDC techniques are infused into the HPC stack and vice-versa.

To aid consistent interpretability across High Performance Computing (HPC) and Big Data Computing (BDC) ecosystems, key concepts

potentially high number of compute nodes. Data is usually partitioned between the nodes, and any data sharing is effected by message exchanges over a high-speed interconnect between the nodes. HPC applications are usually iterative and closely coupled - the underlying mathematical models do cause dependencies between the data blocks owned by different nodes, and this requires frequent communication of data updates (usually of lower-dimensional parts of blocks) between the nodes. As a consequence, the interconnect fabric has to be very fast in terms of bandwidth and latency, essentially turning the entire set of nodes into one single “supercomputer”. This requires expensive high-performance hardware, i.e. high floating-point processing power and very fast (in terms of both latency and bandwidth) network fabric between the nodes. A HPC application operates as a closely coupled and synchronised over many nodes (up to hundreds of thousands) and accesses the data on a storage entity that is attached via the fast network to all the nodes. In effect, such applications use large parts of the system in “exclusive mode”.

There is a clear trend towards innovative approaches that will create significant value by adopting certain techniques of the other.

need to be explicitly explored upfront before addressing the potential of cross stack transfer learning opportunities. We begin by examining the top-level characteristics and objectives for both HPC and BDC stacks (and extending this to related workloads of Machine Learning (ML) and High Performance Data Analytics (HPDA)). Be it on a leadership class supercomputer, small institutional cluster, or in the Cloud - HPC and Big Data Computing (BDC) stacks traditionally have distinct features, characteristics and capabilities.

HPC stacks are designed for modelling and simulation workloads which are compute intense, and focus on the interaction amongst parts of a system and the system as a whole. Typical application areas include physics, biology, chemistry, and Computer Aided Engineering (CAE). HPC targets extremely large amounts of compute operations, which often operate on large sets of data and are executed in parallel on

Big Data Computing stacks are designed for analytics workloads which are data intense, and focus on inferring new insights from big data sets. Typical application areas include search, data streaming, data preconditioning, and pattern recognition. In the case of a Hadoop-type architecture (which is one of the more prevalent ecosystems in Big Data Computing), the data set can be divided into multiple independent sub-problems (i.e. “embarrassingly parallel problems”) and those sub-problems can be solved by multiple “simple” nodes without need for significant communication between processes during the “map” step. Only the “reduce” step requires bringing the results of parallelised parts together.

As the problem size increases, the number of the sub-problems increases accordingly. And as the number of sub-problems grows, the number of simple nodes to solve them also rises. For these architectures, the power lies in having a

huge number of relatively simple nodes (rather than highly tuned nodes as for HPC), which do not have to be tightly coupled. Several applications (or, instances of the same application) run simultaneously on multiple nodes (i.e. opposite to HPC where a single application uses all the nodes in the cluster). Common practices today highlight that HPC uses Batch Queuing system while BDC uses interactive python interfaces – although this difference is diminishing with introduction of newer HPC workloads.

So, in case of HPC workloads we are deploying a single large supercomputer to solve the entire problem. Adding more nodes for running the same problem (“strong scaling”) will initially reduce runtime, yet at a diminishing rate due to the relative increase in communication and coordination overheads, and will later even increase runtime again. To achieve good strong scaling, the performance of the interconnect fabric also has to be improved. In the second case (i.e. BDC), just adding more simple nodes will reduce the amount of work per node, and since much less communication is required between the nodes, also continue to reduce the runtime.

Figure 1 offers a more fine-grained exploration of the respective stacks – presenting a disaggregated profile view for the Supercomputing, Big Data Computing and Deep Learning stacks. We use the term Supercomputing here to denote a specific implementation of HPC, however, many aspects will also apply to institutional clusters. Deep Learning is a Big Data Computing workload that readily stands to benefit from HPC’s experience due to its reliance on (dense) linear algebra, hence we examine it in more detail at this point. Deep Learning (aka artificial neural networks) algorithms typically scale well to produce increasingly better results where larger models can be fed with more data (i.e. Big Data), this in turn requires more computation to train (i.e. more compute is required) – typically using hand-crafted tuning of deep neural networks.



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At ICT 2018, ETP4HPC and BDVA signed a Memorandum of Understanding to officialise their collaboration.

High Performance Data Analytics (HPDA) is not represented in Figure 1 – however architecture-wise, it is close to the BDC column with the Server and Network layers from the HPC column and potentially selected, more highly per-

For Big Data, the power lies in having a huge number of relatively simple nodes that do not have to be tightly coupled, whereas HPC uses highly tuned nodes interconnected by a high performance fabric.

formant communication and I/O services. This “breed” of stack can bring performance and efficiency improvements for large-scale BDC problems, and it could open the door to tackling data analytics problems with inherent dependencies between nodes.

SUPERCOMPUTING (SC)				DEEP LEARNING (DL)			BIG DATA COMPUTING (BDC)			
Middleware & Mgmt	Apps	Boundary Interaction Services			Framework-dependent applications [e.g. NLP, voice, image]			Framework-dependent applications [e.g. 2/3/4-D]		
		Remote desktop [e.g. Virtual Network Computing (VNC)],			Web mechanisms [e.g. Google & Amazon Web Services],			Secure Sockets Layer [e.g. SSL certificates]		
		Secure Sockets Layer [e.g. SSL certificates]			Secure Sockets Layer [e.g. SSL certificates]					
		Domain specific frameworks [e.g. PETSc],			DNN training & inference frameworks [e.g. Caffe, Tensorflow, Theano, Neon, Torch],			Machine Learning (traditional) [e.g. Mahout, Scikit-learn, BigDL],		
		Batch processing of large tightly coordinated parallel jobs [100s - 10000s of processes communicating frequently with each other]			DNN numerical libraries [e.g. dense LA]			Analytics / Statistics [e.g. Python, ROOR, R, Matlab, SAS, SPSS, Sci-Py],		
System SW		I/O libraries [e.g. HDF5, PnetCDF, ADIOS]			Data Storage [e.g. HDFS, Hbase, Amazon S3, GlusterFS, Cassandra, MongoDB, Hana, Vora]			Serialization [e.g. Avro],		
		Data Storage: Parallel File Systems [e.g. Lustre, GPFS, BeeGFS, PanFS, PVFS],						Meta Data [e.g.Hcatolog],		
		Messaging & Coordination [e.g. MPI/PGAs, direct fabric access],			Messaging & Coordination [e.g. Machine Learning Scaling Library (MLSL)]			Data Ingestion & Integration [e.g. Flume, Sqoop, Apache Nifi, Elastic Logstash, Kafka, Talend, Pentaho],		
		Threading [e.g. OpenMP, task-based models]						Data Storage [e.g. HDFS, Hbase, Amazon S3, GlusterFS, Cassandra, MongoDB, Hana, Vora],		
		Conventional compiled languages [e.g. C/C++/Fortran],			Scripting languages [e.g. Python]			Cluster Mgmt [e.g. YARN, MESO]		
Hardware		Scripting languages [e.g. Python, Julia]			Scripting languages [e.g. Python]			Workflow & Scheduling [e.g. Oozie],		
		Domain numerical libraries [e.g. PETs, ScaLAPACK, BLAS, FFTW...],			Batching for training [built into DL frameworks],			Scripting languages [e.g. Keras, Mocha, Pig, Hive, JAQL, Python, Java, Scala]		
		Performance & debugging [e.g. DDT, Vtune, Vampir],			Reduced precision[e.g. Inference engines],			Workflow & Scheduling [e.g. Oozie],		
		Accelerator APIs [e.g. CUDA, OpenCL, OpenACC],			Local distribution layer [e.g. Round robin / load balancing for inference],			Scripting languages [e.g. Keras, Mocha, Pig, Hive, JAQL, Python, Java, Scala]		
		Data Protection [e.g. System AAA, OS/PFS file access control]			Accelerator APIs [e.g. CUDA, OpenCL],					
Apps		Batch scheduling [e.g. SLURM],			Hardware Optimization Libraries [e.g. cuDNN, MKL-DNN, etc],			SVM systems [e.g. Google Sofia, libSVM, svm-py...],		
		Cluster management [e.g. OpenHPC]			LA numerical libraries [e.g. BLAS, LAPACK, etc]			Hardware Optimization Libraries [e.g. DAAL, DPKD, MKL, etc]		
		Container Virtualization [e.g. Docker],			Virtualization [e.g. Dockers, Kubernetes, VMware, Xen, KVM, HyperX],			Virtualization [e.g. Dockers, Kubernetes, VMware, Xen, KVM, HyperX],		
		Operating System[e.g. Linux OS Variant]			Operating System [e.g. Linux (RedHat, Ubuntu, etc), Windows]			Operating System [e.g. Linux (RedHat, Ubuntu, etc), Windows]		

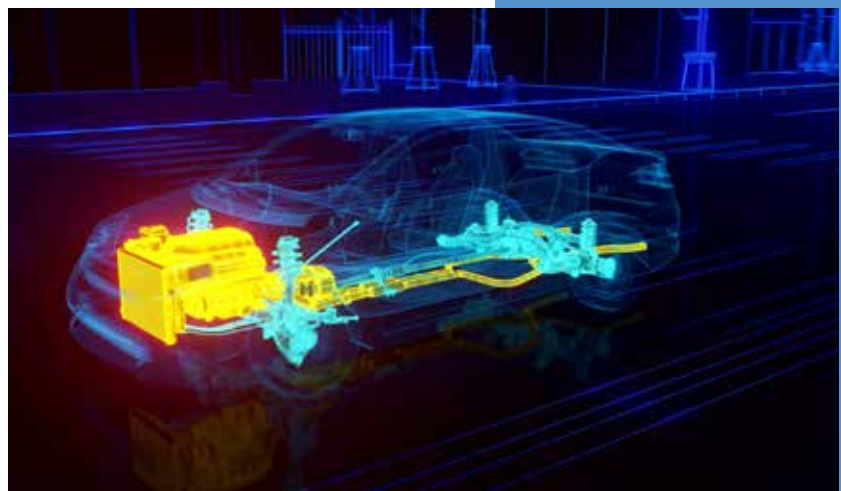


What Big Data Computing can Learn from HPC

Big Data Computing applications are expected to move towards more compute-intensive algorithms to reap deeper insights across descriptive (explaining what is happening), diagnostics (explaining why it happened), prognostics (predicting what can happen) and prescriptive (proactive handling) analysis. HPC capabilities are expected to be of assistance to faster decision making across more complex data sets. As already mentioned, Deep Learning and automated deep neural network design creation are workloads that readily stand to benefit from HPC's experience in optimising and parallelising difficult optimisation algorithms problems. Major requirements include highly scalable performance, high memory bandwidth, low power consumption, and excellent reduced precision arithmetic performance.

What HPC can Learn from Big Data Computing
HPC is now generating models of unprecedented realism and accuracy. At the most extreme, these models represent the real world using trillions of discrete degrees of freedom, which require huge memory and compute performance on extremely large (typically scale-out) systems. These simulations generate enormous amounts of output data. Researchers need to apply advanced and highly complex analytics and processing (including visualisation) to this data to generate insights, which means that off-loading to remote platforms is simply not an option. Thus, data analytics needs to take place in-situ, and perhaps in close coordination with tightly coupled synergistic computing platforms (e.g. visualisation engines). These investigations will have important ecosystem benefits for multi-scale, multi-physics coupled applications, where instances are running on tens to hundreds-of-thousands of nodes.

Therefore, analytics is expected to become a fully-fledged software component of the HPC ecosystem to process the massive results of large numerical simulations or to feed numerical models with complex data produced by scientific and industrial instruments/systems



(e.g. telescope, satellite, sequencers, particle accelerators, etc) or by large scale systems of systems (e.g. edge devices, smart sensors, IoT devices, cyber-physical systems, etc).

In addition, HPC simulations could profit significantly from iterative refinements of their underlying models effected by advanced data analytics tools and machine learning techniques, e.g. by accelerated convergence. HPC can also benefit from Big Data management approaches, especially in the case of dynamic scenarios (Big Data Computing is much more flexible with the notions of data at rest, data on move, data in change). ■

Horizon Europe HPC Vision 2018 Workshops and Future Plans

MARCIN OSTASZ,
ETP4HPC OFFICE

The road mapping efforts of ETP4HPC during the course of Horizon 2020 have been centred on the publication of our Strategic Research Agenda (SRA). Each roadmap outlines the milestones needed to produce competitive HPC technology in Europe. However, there are two paradigms that require us to change that approach.

First, it is clear that HPC will not operate in isolation. While the goals of achieving technological independence by Europe and increasing the global market share of the European HPC technology providers remains valid, we need to work together with other related areas such as Big Data, Internet of Things and Artificial Intelligence in order to be able to deliver the end-to-end solutions required by the European



scientific and industrial user. There is a need, therefore, to expand our thinking and synchronise our objectives with those of the related areas.

Secondly, a new approach is needed to define the scope of our road mapping activities in the new Horizon Europe programme. It is clear that we need to move beyond our classical SRA. We need to figure out where the world is going and in which areas of HPC technology provision and use Europe can excel and achieve long-term leadership.

The HPC Vision document our Association is working on addresses these paradigm shifts.



HiPEAC is a European network of almost 2,000 world-class computing systems researchers, industry representatives and students. It provides a platform for cross-disciplinary research collaboration, promotes the transformation of research results into products and services, and is an incubator for the next generation of world-class computer scientists. It is funded by Horizon 2020.

ETP4HPC and HiPEAC have a long history of collaboration. In 2018, we co-organised a Vision workshop at ISC, as well as a networking session at ICT 2018.

The Vision will set the scene for our work within Horizon Europe. It will form the basis of our next Strategic Research Agendas (SRAs), which will allow EuroHPC to formulate a competitive research programme.

The HPC Vision document our Association is working on addresses these paradigm shifts. The Vision will set the scene for our work within Horizon Europe. It will form the basis of our next Strategic Research Agendas (SRAs), which will allow EuroHPC to formulate a competitive research programme.

The first milestone in the process of preparing the Vision was a workshop we held at ISC 2018 in Frankfurt. We invited world-class HPC experts from Europe, US and Japan and asked



them to share their long-term visions of computing and HPC. Their input was very diverse and daring, ranging from a vision of future use models to new approaches to programming. It is clear that HPC will play an important role in addressing the challenges of the modern world but the main task of our community is to build models for interactions between HPC, Big Data, AI and IoT.

Both BDVA and HiPEAC Visions emphasise the importance of understanding use cases involving HPC, Big Data solutions and end-to-end systems.

In the meantime, two sister organisations – BDVA (Big Data) and HiPEAC (architectures and compilers) – have embarked on a similar effort.

The ICT¹⁸ event in Vienna provided an opportunity to compare the foundations of our HPC Vision with the results of their thinking. Both BDVA and HiPEAC Visions emphasise the importance of understanding use cases involving HPC, Big Data solutions and end-to-end systems. This is in line with the work we have been carrying out together with BDVA, the result of which is a set of scientific and industrial use scenarios. The task ahead of us is to identify the patterns and bottlenecks to be addressed in the future research work.

The Vision document is due by the end of March 2019. In parallel, we are starting to prepare our next SRA. In this process, we will interact closely with EuroHPC to understand its needs and also with the European Processor Initiative in order to facilitate the technologies that turn its results into globally competitive solutions. This work has been supported by the EXDCI and EXDCI2 projects. ■

New Centres of Excellence in computing applications

Ten new Centres of Excellence (CoEs) for computing applications were selected following the 2018 EC call under e-Infrastructures. Their mission: be user-focused, develop a culture of excellence, both scientific and industrial, and place computational science and the harnessing of “big data” at the centre of scientific discovery and industrial competitiveness.

BioExcel, CompBioMed, EoCoE, Esiwace, MaX and POP have been granted funding for a

second phase. They will continue to help strengthen Europe's competitiveness in HPC applications, covering domains such as life sciences, medicine, energy, materials science, or providing services to help scale HPC applications towards exascale. FocusCoE has a transversal mission, supporting the HPC CoEs to more effectively fulfil their role within the European HPC ecosystem and the EuroHPC JU.



Three totally new CoEs are starting, addressing three new domains: geophysics, engineering and multidimensional challenges.

CHEESE

CENTRE OF EXCELLENCE FOR EXASCALE AND SOLID EARTH

ChEESE will address extreme computing scientific and societal challenges by harnessing European institutions in charge of operational monitoring networks, tier-0 supercomputing centres, academia, hardware developers and third-parties from SMEs, Industry and public-governance. The scientific challenging ambition is to prepare 10 open-source flagship codes to solve Exascale problems on computational seismology, magnetohydrodynamics, physical volcanology, tsunamis, and data analysis and predictive techniques, including machine

learning and predictive techniques from monitoring earthquake and volcanic activity. The selected codes will be audit and optimized at both intranode level (including heterogeneous computing nodes) and inter-node level on heterogeneous hardware prototypes for the upcoming Exascale architectures, thereby ensuring commitment with a co-design approach. Preparation to Exascale will consider also code inter-kernel aspects of simulation workflows like data management and sharing, I/O, post-process and visualization.



Coordinator: BSC, Spain

Other Partners:

Atos (Bull SAS), France
CINECA, Italy
CNRS Marseille, France
ETH Zürich, Switzerland
HLRS, Germany
IMO, Iceland
INGV, Italy

IPGP, France
LMU, Germany
NGI, Norway
TUM, Germany
University of Málaga, Spain

www.cheese-coe.eu
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EXCELLERAT

EXCELLERAT is a European Centre of Excellence for Engineering Applications. Several European High Performance Computing Centres teamed up to support several key engineering industries in Europe in dealing with complex applications using HPC technologies. We conduct research, provide leadership, guidance on good practice, user support mechanisms as well as training and networking activities to our community. Our goal is to help Europe leverage scientific progress in HPC driven engineering and address current

economic and societal challenges. The setup of EXCELLERAT complements the current activities of each HPC centre involved and enables the development of next-generation engineering applications. The aim of EXCELLERAT is to support the engineering community at a level that no single HPC provider can.



Coordinator: HLRS, Germany

Other Partners:

ARCTUR DOO, Slovenia
BSC, Spain
CERFACS, France
CINECA, Italy
DLR, Germany
EPCC, United Kingdom
Fraunhofer Gesellschaft, Germany

KTH, Sweden
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SICOS BW GmbH, Germany
SSC-Services GmbH, Germany
TERATEC, France

<https://www.excellerat.eu/>
Twitter: @EXCELLERAT_CoE

HIDALGO

HPC AND BIG DATA TECHNOLOGIES FOR GLOBAL CHALLENGES

Developing evidence and understanding concerning Global Challenges and their underlying parameters is rapidly becoming a vital challenge for modern societies. Various examples, such as health care, the transition of green technologies or the evolution of the global climate up to hazards and stress tests for the financial sector demonstrate the complexity of the involved systems and underpin their interdisciplinary as well as their globality. This becomes even more obvious if coupled systems are considered: problem statements and their corresponding parameters are dependent on each other, which results in interconnected simulations with a tremendous overall complexity. Although the process for bringing together the different

communities has already started within the Centre of Excellence for Global Systems Science (CoeGSS), the importance of assisted decision making by addressing global, multi-dimensional problems is more important than ever. Global decisions with their dependencies cannot be based on incomplete problem assessments or gut feelings anymore, since impacts cannot be foreseen without an accurate problem representation and its systemic evolution. Therefore, HiDALGO bridges that shortcoming by enabling highly accurate simulations, data analytics and data visualisation, but also by providing technology as well as knowledge on how to integrate the various workflows and the corresponding data.



Partners:

ARH Informatikai Zrt., Hungary
Atos Spain, Spain
Brunel University London, United Kingdom
DIALOGIK, Germany
ECMWFs, United Kingdom
HLRS, Germany
ICCS, Greece
Know Center GmbH, Austria

Magyar Kozut Nonprofit Zrt., Hungary
MoonStar Communications GmbH, Germany
PSNC, Poland
Szechenyi Istvan University, Hungary
Universität Salzburg, Austria

8th General Assembly in Ireland



ETP4HPC held its 8th General Assembly on 13 March 2018. Intel Ireland hosted this event in their Leixlip Campus near Dublin, which is home to a semiconductor manufacturing location. The main objective of the event was to elect a new Steering Board. Besides the traditional activity report presented by the Chairman and Treasurer, Michael Malms gave an overview of the core of our activities, the SRA3, and future roadmaps and visions.

The members who joined ETP4HPC in 2017 had the opportunity to introduce themselves to the GA.

Invited speaker Gustav Kalbe (DG Connect) gave an update on the EC's organisation for HPC – a much expected presentation as EuroHPC was only starting to take shape. Finally, a keynote by our host Intel presented their history, research and manufacturing activities in Ireland.

European HPC Summit Week in Ljubljana



This conference organised by EXDCI and co-located with PRACEDays took place from 28 May to 1 June 2018, at the University of Ljubljana (Slovenia). This edition offered a wide variety of workshops covering a number of application areas where supercomputers are key, as well as HPC technologies and infrastructures. It also offered a great opportunity to network with all relevant European HPC stakeholders, from technology suppliers and HPC infrastructures to scientific and industrial HPC users in Europe.

ETP4HPC was very much part of this event, with a keynote by our Chairman Jean-Pierre Panziera, a workshop on Energy efficiency in HPC organized by our Energy Efficiency Working Group, and several speakers among the members of our Steering Board.

Energy Efficiency workshop at European HPC Summit Week



Michael Ott (LRZ), leader of the ETP4HPC Work Group on Energy Efficiency, organised a Workshop on «Energy Efficiency in HPC» on 30 May 2018, within the European HPC Summit Week.

After reporting on the recent activities of the Work Group, Michael Ott gave the floor to four speakers, who each shared with the audience their experience and best practice in terms of energy efficiency.

Axel Auweter, Megware, gave an overview of the 100% Warm-water Cooling solution CoolMUC-3.

Etienne Walter, Atos, representing project Mont-Blanc 3, explained how this project addresses all aspects of energy efficiency, from software to hardware.

Matthias Maiterth, LMU and Intel, introduced the Global Extensible Open Power Manager – GeoPM.

Antonio Libri, ETH, reported on the power monitoring infrastructure installed on the D.A.V.I.D.E. system – derived from work of the MULTITHERMAN project.

Promoting European HPC efforts at Teratec Forum



The Teratec Forum was held on 19-20 June 2018, on the campus of prestigious Ecole Polytechnique near Paris. This conference and exhibition once again brought together the best international experts in HPC, Simulation and Big Data – with more than 1300 attendees representing both the academic community and the industry.

ETP4HPC was one of the 80 exhibitors, sharing a booth with EXDCI. Together we explained and promoted the European efforts to boost the HPC ecosystem.

SME members on our booth at ISC 2018



ETP4HPC was naturally present at Europe's largest HPC event, ISC High Performance, held in Frankfurt (Germany), on 24-28 June 2018.

Just before the start of the conference, we organised a Vision workshop gathering world-class HPC experts from Europe, US and Japan (see report in *Horizon Europe HPC Vision – 2018 Workshops and Future Plans*).

We also had a booth, and this year we had decided to highlight the work of some of our SME members. We hosted Appentra, Asperitas, Iceotope, and Scapos on our booth, giving them visibility in this large event. Following the success of this activity, we will certainly repeat it with a larger booth in 2019!

Birds-of-a-Feather session at SC18



The yearly BoF co-organised by ETP4HPC and EXDCI2 at SC in November has almost become an institution. It was this year entitled «Consolidating the European Exascale Effort» and was held on 14 November in Dallas. We presented to the international HPC community the results of the European Exascale programme to date (covering the entire HPC system stack and application expertise), the ambitions of the new round of basic technology, application, co-design (DEEP-EST/EuroExa), prototype and processor design (EPI) projects, the post-Exascale plans, collaboration with Big Data, IoT and other areas, and a selection of best-performing HPC technology SMEs (Iceotope and Megware), emphasising Europe's global contributions. The session also features a presentation of EuroHPC.

A large audience had the opportunity to exchange with the speakers during the final panel.

All attendees received their copy of the freshly printed 2018 Handbook of European HPC projects - some even took extra copies for colleagues!

Booth at ICT 2018 Conference in Vienna



The ICT 2018 event, co-organised by the European Commission and the Austrian Presidency of the Council of the European Union, was held on 4-6 December 2018 in Vienna (Austria). This large event (6000 attendees) included a conference, an exhibition of EU-funded research and innovation projects in the field of ICT, a series of networking activities, and an Innovation and start-ups village.

ETP4HPC had a booth – strategically located in the main hall, with the PPPs. We presented our Handbook and our Strategic Research Agenda, as well as the production of some of our industrial members (especially SMEs) - innovative pieces of HPC hardware and simulations, whose development was supported by H2020 funded projects.

Full house for our networking session at ICT Vienna



ETP4HPC, BDVA and HiPEAC had joined forces to set up a networking session at the ICT Conference, on 5 December 2018. Under the title “Common priorities of HPC, Big Data and HiPEAC for post-H2020 era”, it aimed to present and get feedback on the common areas of the future technical and strategic research priorities for High-Performance Computing, Big Data and High-Performance Embedded Architecture and Compilation.

ETP4HPC had also been invited to take part to another networking session, as a member of the panel of the Thematic workshop on Artificial Intelligence held on 4 December 2018.

Date	Event	Location	Participation of ETP4HPC
17/01/2018	KPI revision meeting	Brussels, Belgium	JP Nominé for ETP4HPC
09/02/2018	KPI revision meeting	Brussels, Belgium	JP Nominé for ETP4HPC
06/03/2018	Workshop on Digitalising European Industry	Brussels, Belgium	H. Falter attended on behalf of ETP4HPC
12/03/2018	ETP4HPC networking dinner	Maynooth, Ireland	Social event open to all ETP4HPC members
13/03/2018	General Assembly of ETP4HPC	Leixlip, Ireland	General Assembly hosted by Intel Ireland
16/03/2018	ICT Programme Committee	Brussels, Belgium	On invitation by the EC: H. Falter, JP Panziera and JP Nominé representing ETP4HPC
20/03/2018	Workshop on SMEs and the uptake on HPC	Brussels, Belgium	On invitation by the EC: H. Falter for ETP4HPC and M. Gilliot on behalf of EXDCI
27-28/03/2018	BDECng meeting	Chicago, USA	on invitation by the US colleagues: JP Panziera for ETP4HPC
17-19/04/2018	EASC: Exascale Applications and Software Conference	Edinburgh, Scotland	
19/04/2018	Shaping Europe's Digital Future: HPC for Extreme Scale Scientific and Industrial Applications	Sofia, Bulgaria	JP Panziera and JP Nominé representing ETP4HPC
25-26/04/2018	Joint Workshop ETP4HPC - BDVA on use cases	Brussels, Belgium	Led by Michael Malms for ETP4HPC
27/04/2018	EXDCI Final Review	Luxembourg, Luxembourg	ETP4HPC represented by Marcin Ostasz (WP2) and Maïke Gilliot (WP7)
04/05/2018	EuroHPC meeting with EC	Luxembourg, Luxembourg	Jean-Pierre Panziera, Jean Gonnord and Hugo Falter representing ETP4HPC
14-15/05/2018	Open eIRG Workshop	Sofia, Bulgaria	Marcin Ostasz representing ETP4HPC
17/05/2018	ENES/ESIWACE HPC Workshop	Lecce, Italy	Thomas Eickeman representing ETP4HPC (talk on SRA and EsDs)
28/05/2018 01/06/2018	European HPC summit week	Ljubljana, Slovenia	Events and Workshops (co-) organised by ETP4HPC
28/05/2018	EXDCI Workshop	Ljubljana, Slovenia	As part of the HPC Summit Week
29/05/2018	cPPP Partnership Board meeting	Ljubljana, Slovenia	During the HPC Summit Week
30/05/2018	Workshop of the Energy Efficiency Workgroup	Ljubljana, Slovenia	As part of the HPC Summit Week
13/06/2018	EuroHPC WG on "User Requirements"	Brussels, Belgium	Jean-Philippe Nominé representing ETP4HPC
19-20/06/2018	Forum Teratec	Palaiseau, France	Booth at the Teratec Exhibition
24-28/06/2018	ISC	Frankfurt, Germany	Booth at the ISC-Exhibition
24/06/2018	Open Workshop to all members on FP9 position paper	Frankfurt, Germany	during ISC 18
27/06/2018	Closed Workshop on FP9 position paper	Frankfurt, Germany	during ISC 18
03/07/2018	EuroHPC workshop on SMEs and the uptake of HPC (2 nd Workshop)	Brussels, Belgium	Maïke Gilliot representing EXDCI and ETP4HPC
10/07/2018	cPPP Review: 2017 PMR	Brussels, Belgium	Jean-Philippe Nominé and Guy Lonsdale for ETP4HPC
13/07/2018	EuroHPC preparation: joint meeting ETP4HPC- BDVA - EC	Brussels, Belgium	Jean-Pierre Panziera, Hugo Falter and Jean Gonnord representing ETP4HPC
01/08/2018	cPPP : KPI review and PMR 2017 discussion	Brussels, Belgium	Maïke Gilliot representing ETP4HPC
27/09/2018	EXDCI-2 First technical meeting	Brussels, Belgium	Marcin Ostasz representing ETP4HPC
02/10/2018	Portes Ouvertes Teratec	Bruyères le Châtel, France	Booth
23/10/2018	cPPP meeting	Brussels, Belgium	
30-31/10/2018	PRACE-CoEs-FET HPC-EXDCI Workshop	Brühl, Germany	Marcin Ostasz representing ETP4HPC
14/11/2018	Big Data Value Forum (BDVA)	Vienna, Austria	Michael Malms in Panel
14/11/2018	SC BoF	Dallas, Texas, US	
04-06/12/2018	ICT event	Vienna, Austria	Booth
05/12/2018	ICT event: Joint ETP4HPC-BDVA Networking Session - Public Review of post-H2020 Vision	Vienna, Austria	