ExaNoDe core technologies towards Extreme-Scale Demonstrators

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ExaNoDe Project

ExaNoDe is about compute node aiming:
- Energy Efficiency.
- Dense Integration.
- Affordability.

ExaNoDe Core Technologies for compute node:
- ARMv8 based architecture.
- Integration technologies:
  - 3D integration/chiplet/interposer
  - Multi-chip-Module
- Virtualisation of system and resources:
  - Global Address Space (UNIMEM)
  - Virtualisation

ExaNoDe objectives:
- To validate the ExaNoDe core technologies as enablers for European exascale HPC in an appropriately balanced integrated PoC solution.
- To deliver a compute node integrating core technologies consistent with the HPC system sizings and requirements for exascale computing.

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Project Implementation

T0: October 1\(^{st}\), 2015:
ExaNoDe @ Month 8

Coordinator

CONSORTIUM

IMPLEMEN-
TATION

PROOF-OF-CONCEPT

WP1: Management

WP2: Co-Design for Exa-scale HPC systems

WP3: Enabling of Software Compute Node

WP4: Compute node design and manufacture

WP5: System Integration & Evaluation

WP6: Dissemination and Exploitation

8.6 M€

12.05.2016

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HORIZON 2020

Compute Node

ExaNoDe prototype

ExaNoDe SW stack

Balanced mini-apps
Virtualization
Parallel programming
OS, Firmware

Manchester
ExaNoDe realisation: Proof-of-Concept

Integrated Proof-of-Concept

Architecture: ARMv8, UNIMEM

Integration technology: active interposer and related design IPs in chiplet

Integration technology: Multi-chip-Module

Performance analysis

Critical kernel from mimi-apps

Prototype roadmap

SW stack

SW stack

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ExaNoDe role in the Extreme Scale Demonstrators

- Core technology provider for HPC system architecture and components:
  - System architecture:
    - Many-core architecture,
    - Heterogeneous architecture,
    - Memory management policies.
  - Components:
    - Integration technologies: active interposer, Multi-Chip-Module,
    - Design enablement solutions: libraries, IPs, methodologies.
  - Software enablement solutions:
    - Firmware and OS,
    - Virtualisation,
    - Parallel programming models and runtime libraries.
- Evaluated in the context of HPC mini-applications with ExaNoDe PoC.

➢ To go toward an integrated compute node beyond the FPGA-version planned in the PoC.
Topics to be addressed

- Chiplet
- Interposer
- Memory
- Scalability, interconnect, storage, cooling
- HW acceleration
- Shared I/O
- 3D & MCM integration
- SW stack and programing environment

Example of Next Generation of Compute Node based on ExaNoDe core technologies and targeting TRL 7-8
ExaNoDe Technologies Deployment

Chiplet:
- Architecture: ExaNoDe
- Design of interface: ExaNoDe
- Design of computing part:
- Manufacturing:

Memory:
- Multi-Chip-Module integration: ExaNoDe
- I/O bandwidth:
- Samples:

3D & MCM integration

Interposer:
- Architecture: ExaNoDe
- Design:
- Manufacturing & test: ExaNoDe

SW stack and programming environment: ExaNoDe

Example of Next Generation of Compute Node based on ExaNoDe core technologies and targeting TRL 7-8

Scalability, interconnect, storage, cooling

HW acceleration:
- FPGA samples
- FPGA design

Shared I/O
Chiplet:
- Architecture: ExaNoDe MONT-BLANC
- Design of interface: ExaNoDe
- Design of computing part:
- Manufacturing:

Interposer:
- Architecture: ExaNoDe ExaNoDe
- Design: ExaNoDe
- Manufacturing & test: ExaNoDe

Memory:
- Multi-Chip-Module integration: ExaNoDe
- I/O bandwidth:
- Samples:

Example of Next Generation of Compute Node based on ExaNoDe core technologies and targeting TRL 7-8

Scalability, interconnect, storage, cooling

HW acceleration:
- FPGA samples
- FPGA design

Shared I/O

SW stack and programing environment:
Still Missing?

Chiplet:
- Architecture: ExaNoDe MONT-BLANC
- Design of interface: ExaNoDe
- Design of computing part: ?
- Manufacturing: ?

Interposer:
- Architecture: ExaNoDe ExaNoDe
- Design: ExaNoDe
- Manufacturing & test: ExaNoDe

SW stack and programing environment:
ExaNoDe MONT-BLANC

Example of Next Generation of Compute Node based on ExaNoDe core technologies

Memory:
- Multi-Chip-Module integration: ExaNoDe
- I/O bandwidth: Nextgenio
- Samples: ?

Scalability, interconnect, storage, cooling

HW acceleration:
- FPGA samples ?
- FPGA design

Shared I/O

ExaNoDe MONT-BLANC
Conclusion

- As individual, it’s difficult for a project to reach a fully integrated HPC prototype targeting TRL 7-8.

- Combining isolated R&D outcomes from different projects is essential.

- At compute node level, don’t forget to address:
  - System architecture among projects,
  - Rocketing cost of processor design and manufacturing with advanced technologies,
  - European dependency on memory and FPGA procurements.
Thank you!

European Exascale Processor & Memory Node Design

www.exanode.eu