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EUROLAB-4-HPC

Eurolab-4-HPC Roadmap

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Technion Israel Institute of Technology

20/3/2017

Agenda

- EuroLab-4-HPC
- Roadmap Scope, Organisation and Status
- EuroLab-4-HPC Roadmap Topics
- Discussion

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Mission: EuroLab-4-HPC will join HPC Systems Research in Europe

EuroLab-4-HPC: H2020-FETHPC-2014, Budget €1.5 M, Sep 2015 to Aug 2017

Gap

- Key HPC stakeholder community (research, suppliers, venture capital) is fragmented and uncoordinated
- Uncoordinated research community

What is needed is

- Join research and other stakeholders around a common long-term research agenda
- Train future technology leaders
- Accelerate innovation

Vision: A European HPC systems virtual Centre of Excellence

Universität Augsburg University · Barcelona Supercomputing Center · The University of Edinburgh · EPFL École Polytechnique Fédérale de Lausanne · ETH · Universiteit Gent · HLRS · FORTH Institute of Computer Science · INRIA · Manchester 1824 The University of Manchester · RWTH Aachen · Technion Israel Institute of Technology

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Objectives

- **Join HPC system research groups** around a long-term HPC research agenda by forming an HPC research roadmap and joining forces behind it
- **Define an HPC curriculum** in HPC technologies and best-practice education/training methods to foster future European technology leaders
- **Accelerate commercial uptake** of HPC technologies
- **Build links** between the HPC research community and other stakeholders (suppliers, venture capital, etc.)
- **Form a business model** and organization for a future Centre of Excellence on HPC systems

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EUROLAB-4-HPC ROADMAP

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Roadmap Scope

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- Long-term vision for excellence in European HPC research
- Beyond Exascale targeting 2022—2030
- Include all layers of HPC stack
  - From applications to hardware
  - Covering disruptive technologies
  - And adjacent domains: high-perf. embedded, data centres, big data
- Close collaboration with other roadmaps
  - HiPEAC Vision
  - ETP4HPC SRA
- Preliminary roadmap (August 2016)
  - https://www.eurolab4hpc.eu/roadmap/
- Final roadmap (August 2017)

Preliminary Roadmap Approach

- Because targeting 2022-2030 is highly speculative:

1. Select disruptive technologies that may be technologically feasible in the next decade
2. Assess the potential hardware architectures and their characteristics.
3. Assess what that could mean for the different HPC aspects.

The preliminary roadmap follows the structure:
"IF technology suitable
THEN foreseeable impact on WG topic could be"

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The 5+1 Working Groups

WG0: Disruptive Technologies (leader: Theo Ungerer, U. Augsburg)

WG1: New technologies and hardware architectures (leader: Avi Mendelson, Technion, Haifa)

WG2: System software and programming environment (leader: Paul Carpenter, BSC, Barcelona)

WG3: Vertical challenges: Green ICT, energy and resiliency (leader Axel Tenschert, HLRS, Stuttgart)

WG4: HPC applications: evolution and requirements (leader: Paul Carpenter, BSC, Barcelona)

WG5: Convergence of embedded HPC, data centers for big data, and HPC (leader: Babak Falsafi, EPFL, Lausanne)

Disruptive Technologies

- **Sustaining Technology** (improving HPC HW in ways generally expected)
  - Continuous CMOS Scaling
  - Die Stacking - 3D-Chip
- **Disruptive Technology in Hardware/VLSI** (innovation that creates a new line of HPC HW superseding existing HPC techniques):
  - Non-volatile Memory (NVM) Technologies
  - Photonics
- **Disruptive technology** (alternative ways of computig)
  - Resistive Computing
  - Neuromorphic Computing
  - Quantum Computing
- **Beyond CMOS**
  - Nanotubes
  - Graphene
  - Diamond

Improving the Preliminary Roadmap

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- Preliminary roadmap deliverable was well received
  www.eurolab4hpc.eu/roadmap/
- EC Reviewer Comments
  - Enhance with proposals of what EC should be funding
  - Integrate/combine with EXDCI SRA: see later slide
- Other observations
  - Working groups proved not very effective
  - WG sections in preliminary roadmap not well aligned with each other

Recommendation from EC: Collaboration with ETP4HPC

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- [R5] As for WP2 it is encouraged to **produce a single roadmap in Europe** in **collaboration with EXDCI**, especially since the project addresses areas that are not addressed by the others […].

- We do not believe that a single EXDCI+EuroLab roadmap is feasible
- But what could be done to address this recommendation?
  - 1) Avoid unnecessary contradictions – understand how differences relate to different aims
  - 2) Add paragraph to EuroLab-4-HPC roadmap and ETP4HPC SRA explaining relationship and differences with other roadmaps, including each other?
  - 3) Add download link on each website to the other roadmap?
  - 4) Joint dissemination strategy? (promote each other's news, etc.)

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Mission for Second Year

- Form single expert working group
  - Currently Avi Mendelson, Luca Benini, Babak Falsafi, Sandro Bartolini, Dietmar Fey, Marc Duranton, François Bodin, Simon McIntosh–Smith, Igor Zacharov, Paul Carpenter, Theo Ungerer
- Revisit Disruptive Technologies and implications of current roadmap
- Harmonize and revise the different roadmap sections
- Recommend potential EC funding opportunities
- Portfolio of a virtual EuroLab-4-HPC Centre of Excellence on European HPC systems research

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Schedule for Second Year

- 2017-03-17: Kickoff Telco of expert working group
- **2017-03-20: Discuss at ETP4HPC SRA Kickoff**
- 2017-04-27/28 at HiPEAC CSW Zagreb: half day preliminary discussions of experts and Eurolab-4-HPC partners
- 2017-05-17 at HPC Summit:
  - 9 to 10:30: meeting with experts and key participants of ETP4HPC and PRACE
  - 14:30-18:30: Roadmapping talk at Workshop of EuroLab-4-HPC: the Future of High-Performance
- 2017-05-29+30 : 1½ day Roadmap meeting of expert working group at EPFL Lausanne
- 2017-06: Experts prepare inputs
- 2017-07-31: Final Roadmap done
- **2017-08-31: Final Roadmap deliverable due**
- 2017-09-08: Joint EXDCI + EuroLab-4-HPC session at ACM Europe Conference

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Main Open Technical Questions

- How will large non-volatile memory impact HPC applications and software?
  - Storage class memory may fill the gap between memory and flash/disc drive
- How to use new technologies in software (NVM, 3D stacking, neuromorphic, accelerators)
- Evolution of MB/core, memory & interconnect BW and latency, …
- What are disruptive ideas in software and applications?
- Any use for special-purpose accelerators like resistive computing (near memory), neuromorphic computing, quantum computing?