Conclusions of sixth cPPP Partnership Board meeting

Brussels, 8 November 2016

- **Welcome by Co-Chairs (ETP4HPC, EC)**

Thomas Skordas (TS) and Jean-Francois Lavignon (JFL) introduce participants, including CoE coordinators.

- **Update on ETP4HPC (ETP4HPC)**

Change of representation in Bull/Atos before next General Assembly : JFL replaced by Jean-Pierre Panziera. JFL will leave his role as chairman of the platform.

ARM is listed as international company after Softbank take-over and stays on the steering board.

- **Presentation of the results of the call FET HPC 01 2016 (EC)**

Andrea Feltrin presents the scope, contents and the response to the FETHPC-2016 call.

- **Time frame for WP2018-2020 – New versions of SRA (EC and ETP4HPC)**

TS explains new organisation chart of DG CNECT and proposes to share it with ETP4HPC (sent). TS summarizes funding of HPC in WP 18-20, which is first priority for Directorate C on Digital Excellence and Science Infrastructure. IPCEI is being developed with MS and is positioned between HPC, data analytics and cloud. Pre-notification to DG COMP ready by early 2017, full notification to follow a few months later. JFL asks to update ETP4HPC when more information about the pre-notification is available.

Leonardo Flores Añover (LFA) presents WP 18-20 outlook.

JFL presents ETP4HPC proposal for WP 18-20. He does not expect a big impact from ongoing and future RIAs on 2020 procurement; instead the work done in RIAs will be harnessed in the 2023 procurement. ETP4HPC will deliver first recommendations before Christmas and refine them by the end of January taking into account the mapping of FETHPC-2014 proposals to the SRA and the outcome of FETHPC-2016, if available. LFA suggests to have a workshop soon to pin down more details about content and timeline (meeting organised for 5 December 2016).

- **Centres of Excellence – considerations for next call (EC and ETP4HPC)**

LFA presents ideas for 2nd Call on CoEs, expected in 2018.

Erwin Laure presents a view built using a consultation of CoES. The second call should consolidate running projects and address new areas, e.g. engineering, fundamental physics

and environmental disaster prevention. CoE calls should be timed early 2018 so that EsD consortia know the outcome before submitting their proposal later that year. CoEs on transversal topics like big data, application sustainability and math could be considered. Addressing the sustainability of CoEs will not be easy, especially if they focus on exascale, where industry interest is limited. Indicative budget for the projects should be 10-20M€. The total budget needed estimated by ETP4HPC is 85 m€.

- **Presentation and discussion on large integrators (EsD)**

Thomas Eickermann presents EsD concept. EXDCI organized in Barcelona on Sept 22nd a workshop with 8 system integrators (of which 4 European) to discuss the EsD concept. All expressed interest, especially for the co-design with leading European scientific and industrial application developers. They are willing to drive the development of system architectures if there is a clear opportunity for commercial exploitation. The 2 EsD calls are presently timed to start towards the end of FETHPC-2014 and FETHPC-2017 projects that develop the exa-scale technology building blocks. Integrators consider that an analysis/exploration preparation phase of 6 months in 2017 could be beneficial to understand how to incorporate the project results in the first EsD call. So far, these projects have been involved on two occasions to contribute to the EsD concept: in May 2016 at the European HPC Summit and in June 2016 at ISC. However, a framework for this preparation is missing.

Work in phase A of EsDs is mostly geared towards engineering for integration with relatively little research. Duration of 2 years is deemed sufficient for that, conditional to the preparation phase in 2017 mentioned above. ETP4HPC has analysed 3 different funding options for EsDs: PCP+PPI, public procurement and purchase by system integrator within a RIA. ETP4HPC has a preference for the third option, because first one is too long and the second one is too risky. Also, a process that favours the selection and funding of EsDs developing architectures for different types of workloads would be beneficial.

TS points out that there should be a way to have BDVA enter the EsD picture and encourages the ETP4HPC to set up a workshop.

- **Yearly reporting on PPPs (finalisation of 2015 and timeframe for 2016) (EC and ETP4HPC)**

Jean-Philippe Nomine (JPN) presents the work on the 2015 cPPP yearly report. ETP4HPC would like to see other reports for benchmarking and improving the 2016 report due by end of March 2017. EC to report to ETP4HPC review results as soon as available. TS anticipates that first feedbacks include a critical review of the KPIs, clarification on the leverage factor and the importance to collaborate with other cPPPs like BDVA.

- **International cooperation (all)**

JFL presents international cooperation, mainly through BDEC. Collaboration with Japan has no clear progress, but in general it would be good to maintain the relationship. EM points out synergies with Japanese groups for application developments.

- **Communication-PR events including SME award discussion (all)**

Marcin Ostasz presents dissemination plans and an idea for an SME award in HPC. EC confirms that if the prize award is not large, it can be supported by EXDCI.

JPN says that the European HPC summit is planned for 15-19 May 2017 in Barcelona, hosted by BSC.

- **AOB and Next meeting**

The status of the IMCO draft report on HPC is discussed. TS stresses that the situation is under control and that the ITRE report is more relevant. TS encourages the ETP4HPC to inform MEPs.

Next meeting will take place during the European HPC Summit in May 2017, Wednesday 17 May from 9h to 12h30.