Exploiting eXascale Technology with Reconfigurable Architectures

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Reconfigurable Technology Basics

CPU

Application Software

Reconfiguration Request

Configuration Manager

config. DB

Static

FPGA

F2

Configuration Interface
Reconfigurable Technology Basics

Technology for practical adaptable hardware systems
• Can **add/remove** components at **run-time/product lifetime**
  – Hardware can change post deployment
• **Flexibility** at hardware speed (not quite ASIC)
• **Parallelism** at hardware level (depending on application)
• Ideally: alter function & interconnection of blocks

Implementation in:
• **FPGAs**: fine grain, complex gate + memory + DSP blocks
• **Coarse Grain** (custom) chips: multiple ALUs, multiple (simple) programmable processing blocks, etc.
The EXTRA Project

- Exploiting eXascale Technology with Reconfigurable Architectures
- Main objective:
  - Develop an open source research platform for continued research on reconfiguration architecture and tools
- Develop and program HW with run-time reconfiguration as a design concept
- Enable joint optimization of architecture, tools, applications and reconfigurable technology
- Prepare the HPC hardware nodes of the future

Fits Extreme-Scale Demonstrator
Demonstration and Use

• Demonstrate the effectiveness of the EXTRA platform for developing three complex applications from different application domains:
  – (a) Financial option pricing application (Maxeler)
  – (b) Retinal image segmentation (Synelixis)
  – (c) scientific applications: Quantum Monte Carlo (University of Cambridge)

• Evaluate the open research platform for reconfiguration and promote it to other researchers.
  – First contact with Research Advisory Board (RAB) and Industry Advisory Board (IAB) planned next month

Extreme-Scale Demonstrator could benefit from this platform
EXTRA partners

- Universiteit Gent
- Politecnico Milano 1863
- Imperial College London
- University of Amsterdam
- MAXELLE Technologies
- Synelixis

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