ETP4HPC
Extreme Scale Workshop
HPC Summit Prague, May 12th 2016
Agenda

• 9:00 Welcome (SRA Editorial team)
• 9:10 EsDs - main directions and assumptions (Thomas Eickermann and Marc Duranton)
• 9:30 EsD concept – the view of the EC (Dr. Panagiotis Tsarchopoulos)
• 9:40 Project/Organisation Presentations – Part 1
• 10:40 Coffee Break
• 11:00 Project/Organisation Presentations – Part 2
• 12:30 Lunch
• 13:15 Interactive session (2 x 40min min discussion sessions per “table”):
  • Technical total system target characteristics (facilitator: Marc Duranton)
  • Required ESD project budget assumptions (facilitator: Hans Christian Hoppe)
  • Procurement model options (facilitator: Dirk Pleiter)
  • Composition of consortia - roles and tasks, e.g. of SMEs and appl. Owners (facilitator: Thomas Eickermann)
  • Use Cases Enabled by EsDs (facilitator: Erwin Laure)
• 15:00 Result of the interactive sessions
• 1550 Next steps
• 16:00 End
Flow of interactive session

- 5 “focus tables” with 2 x 40 min discussion sessions:
  - Each participant can take part in two different discussion in the 1st and 2nd round
  - Participants have put their names down for the desired team for both rounds

- For each 40 min round:
  - Each team should nominate a **Spokesperson** summarising the results at the end
  - Flipcharts should be used to document questions/results/recommendations
  - There is a **Facilitator** appointed for each topic (**they do not change tables**)
  - Groups will be split into smaller teams because of their size
  - After the first 20 min the sub-teams should merge their statements (which should take 20 min as well)

- After the second session each Spokesperson should present the results at the end of the session
  - 5 min maximum
  - Send us (**office@etp4hpc.eu**) an email with their summary!!!!
Main directions and assumptions

• “The “Extreme-Scale Demonstrators” (EsDs) are vehicles to optimise and synergise the effectiveness of the entire HPC H2020 Programme through the integration of isolated R&D outcomes into fully integrated HPC system prototypes; It is a key step towards establishing European exascale capabilities and solutions.”  
(From the ETP4HPC SRA, chapter 8 p.67)

• “Integrate technologies into system prototypes, co-designing solutions and procuring HPC systems; the resulting HPC infrastructure will focus on supercomputers of top-range capabilities connected to mid-range EU national computing centres and to pan-European data and software infrastructure to offer supercomputing as a service”

• The Commission and participating Member States should develop and deploy a large scale European HPC, data and network infrastructure, including:
  – the acquisition of two co-designed, prototype exascale supercomputers and two operational systems which will rank in the top three of the world;
(From the EC Communication “European Cloud Initiative - Building a competitive data and knowledge economy in Europe”
EsD State of Play

• EsD concept is outlined in the latest ETP4HPC SRA
• Next SRA will provide more details:
  enable cPPP to propose concrete calls
• Aim of this Workshop: gather community input for next SRA
  – Main EsD characteristics and performance targets
  – Defining a suite of challenging pre-exascale problems / examples of possible applications
  – Options for funding and project implementation – timetable
  – Also: “Marriage Market” for parties interested in participating to the EsD calls
• Next steps
  – Digest results from workshop
  – Continue discussion at future events, e.g. SRA workshop at ISC in June
EsD proposal calls

• Two set EsD calls, each leading to two projects
  – Calls target technologies developed under FETHPC, but are open
  – EsD projects should start after end of FETHPC projects in WP2014/15 and WP2016/17

• EsD project structure
  – **Phase A** (18-24 months): Development, Integration and Testing
    • Little or no basic technology research
    • Substantial R&D focus geared towards integrating components and sub-systems developed in the preceding R&D projects
  – **Phase B** (18-24 months): Deployment and Use
    • Operated by a hosting center
    • EsD made available to application owners for code porting and development
    • Characterization and EsD validation, benchmarking based on real use-cases.
HPC-Horizon 2020 roadmap

---|---|---|---|---|---|---|---|---|---|---
WP 14/15 | | | | | | 100M | | | | |
start of projects

WP 16 | | | | | | 100M | 2018
SRA1 - update

WP 17 | | | | | | 45M | | | | |
SRA2.0

WP 18/19 | | | | | | 180M
SRA 2.0 update

WP 20/21 | | | | | | 120M
SRA 3.0

CSA 14/15: EXDCI | 9/2015 | | | | | |
start of call

CSA 16/17: EXDCI | | | | | | 8/2020

Extreme scale Demonstrators

EsD 1-2 projects

EsD 3-4 projects

WP 17 | | | | | | 45M
SRA2.0

EsD call

EsD integration

EsD deployment & use

EsD call

EsD integration

EsD deployment & use

EsD call

EsD integration

EsD deployment & use

ESGA 14/15: EXDCI
9/2015

2/2018

SRA 1 - update

SRA 2.0 update

SRA 3.0

version 5.1
Assumptions / Fixed Points

- Diversity of System Architectures
- Design points must be pre-exascale (~400-500 PFLOPS) with a target of 5% (20-30 PFLOPS) installed and tested
- Phase A (integration) and Phase B (deployment) treated as ONE project
- Each EsD project consortium is composed of
  - Technology providers (HW, SW)
  - Application providers - e.g. CoE
  - Hosting HPC centres
  - At least one system integrator
  - At least one global system architect
- Application development outside of funding scope
Timetable for Interactive Session

- **13:15** INTRO Interactive session (2 x 40min min discussion sessions per “table”):
  - **13:25** Start of Round 1 – Small team discussion
  - **13:45** Merger Sessions of each table (joining the small teams)

- **14:05** Participants change tables for round 2
  - 10 min ..... 
- **14:15** Start of Round 2 – Small team discussion
- **14:35** Merger Sessions of each table (joining the small teams)

- **14:55** Tables join in Meeting room

- **15:00** Result of the interactive sessions (5 min per session chair)
- **15:50** Wrap up, Next steps
- **16:10** End
Tentative Questions for Table Discussions (1/3)

• Technical: total system target characteristics
  – Which characteristics to look at?
    Flops, Flops/W, memory bandwidth/capacity, interconnect, scalability, reliability/resiliency, level of specialization, programming model, ... ?
  – Which “personalities” could the 4 EsDs target?

• Budget: required ESD project budget assumptions
  – Is the currently proposed funding envelope appropriate (ETP4HPC recommends 4 x 50 M€) ?
  – What would be a typical split of funding among activities in the project?
  – Is the currently proposed timeline realistic?
Tentative Questions for Table Discussions (2/3)

• Procurement: model and options
  – Suitability of standard and new procurement models for EsDs?
    PPI, Innovation partnership, ...
  – How to ensure buy-in of HPC centres?
  – Potential conflict of roles?
    centres & integrators as procuring entity & provider AND as project partners
  – Potential conflict of objectives?
    leverage results from H2020 HPC programme & fair and open competition

• Composition of consortia – roles and tasks
  – Who could act as coordinator (HPC centre, integrator, ...)
  – How to ensure buy-in of application communities?
  – Which role can SMEs play?
  – How to ensure a transition from EsDs to products?
Tentative Questions for Table Discussions (3/3)

• Use Cases Enabled by EsDs
  – What use cases could be enabled with the help of an EsD?
  – Which features and capabilities are required to make an EsD suitable for this use case?
  – How long must the EsD be available to achieve the use case goal?
  – Which software/hardware technologies developed with support from FP7/H2020 funding could be of particular interest?
THANK YOU!

For more information visit

www.etp4hpc.eu

contact: office@etp4hpc.eu
Backup
Contribution / Role of Participants

**Technology providers**
- Technology integration
- Project management
- Testing and quality/performance assurance (phase A)
- Maintenance and service (phase B)

**Application owners / CoEs**
- Application requirements and key challenges (phase A)
- Port, optimize application(s), use them productively (phase B)

**EsDs**

**HPC Centres**
- Participate in co-design
- Manage system deployment (phase A)
- System operation, validation (phase B)