ETP4HPC
Strategic Research Agenda (SRA)
HiPEAC Conference, January 2016
Introduction

HPC EC plan
The Main **Objective** of ETP4HPC

“To build a globally competitive European world-class HPC technology value chain”
ETP4HPC members

- **71** organizations involved in HPC technology research based in Europe:
  - 36 companies (22 SMEs)
  - 31 RTOs + 2 others

- Full members: 48
A bit of history

- 2004: first attempts at designing and building a European HPC Research Infrastructure (HPCEUR, HET), which resulted in the creation of PRACE in 2010

- 2010: meetings of experts representing EC and European stakeholders to define a global policy

- 2011: the creation of ETP4HPC

- Actions in FP7
  - PRACE Preparatory Phase and first Integrated Projects
  - Supports action : EESI and EESI2
  - Calls for Exascale computing in WP2011 and WP2013
The EC Communication

- High-Performance Computing: Europe's place in a Global Race issued in Feb 2012
- Policy based on 3 pillars

Access to best HPC for industry and academia (PRACE)
- Collaboration of HPC Centres and application CoEs
- Provision of HPC capabilities and expertise

Excellence in HPC applications (Centres of Excellence)

FET/HPC: EU development of Exascale technologies
- Specifications of exascale prototypes
- Technological options for future systems
- Identify applications for co-design of exascale systems
- Innovative methods and algorithms for extreme parallelism of traditional/emerging applications
The HPC Public Private Partnership

• Mutual commitment
  – European Commission
    • HPC as a priority in Horizon2020
    • Funding of 700 M€
  – ETP4HPC
    • Investment to match EC funding in R&D
    • Effort to maximise impact on European industry

• Partnership board
  – strategy setting
  – impact monitoring
Support actions

• EESI and EESI2
  – run by European experts from 2008 to 2015
  – important recommendations covering technology, applications, algorithms
  – http://www.eesi-project.eu/

• EXDCI
  – managed by PRACE and ETP4HPC
  – started in Sept 2015
  – supporting:
    • roadmap: technical (SRA), scientific cases
    • cross cutting topics: technical topics, training, SMEs
    • international cooperation
    • monitoring
The Horizon 2020 HPC projects

• First call of Horizon2020
  – 19 research projects and 2 support actions
  – Most projects started in Sept-Oct 2015 for 3 years
  – Total effort : 94 M€ for R&D projects

• Summary:
  – 170 organisations involved in this effort
  – Project distribution
    • 9 HPC core technologies and architectures
    • 5 Programming methodologies, environments, languages and tools
    • 0 APIs and system software
    • 5 New mathematical and algorithmic approaches

<table>
<thead>
<tr>
<th>Sector</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Industry</td>
<td>15.7%</td>
</tr>
<tr>
<td>Non EU</td>
<td>0.2%</td>
</tr>
<tr>
<td>Research</td>
<td>68.9%</td>
</tr>
<tr>
<td>SME</td>
<td>15.3%</td>
</tr>
</tbody>
</table>
More in progress

- 2 calls in Work Programme 2016-2017
  - FET HPC 1 2016: Co-design of HPC systems and applications
  - FET HPC 2 2017: Transition to Exascale Computing
    - 5 subtopics:
      - High productivity programming environments for exascale
      - Exascale system software and management
      - Exascale I/O and storage in the presence of multiple tiers of data storage
      - Supercomputing for Extreme Data and emerging HPC use modes
      - Mathematics and algorithms for extreme scale HPC systems and applications working with extreme data
    - budget: 40 M€ - deadline: 26 September 2017
- On-going discussion on additional Horizon2020 programme
- New HPC initiative by the European Commission
Strategic Research Agenda
SRA
a multi-annual roadmap towards Exascale High-Performance Computing Capabilities
Horizon 2020 WP and SRA
Priorities

• There is a demand for R&D and innovation in both extreme performance systems and mid-range HPC systems
  – Scientific domain and some industrial users want extreme scale
  – ISVs and part of the industry expect more usability and affordability of mid-range system

• The ETP4HPC HPC technology providers are also convinced that to build a sustainable ecosystem,
  – their R&D investments should target not only the exascale objective (too narrow a market)
  – an approach that aims at developing technologies capable of serving both the extreme-scale requirements and mid-market needs can be successful in strengthening Europe’s position.
4 dimensions of the SRA

- **HPC SYSTEM ARCHITECTURE**
- **SYSTEM SOFTWARE AND MANAGEMENT**
- **PROGRAMMING ENVIRONMENT** Including: Support for extreme parallelism
- **MATHEMATICS & ALGORITHMS FOR EXTREME SCALE HPC SYSTEMS** — NEW —

**HPC SERVICES INCLUDING:** ISV support, End-user support

**SME FOCUS**

**EDUCATION AND TRAINING**

**HPC STACK ELEMENTS**

**HPC USAGE EXPANSION**

**EXTREME SCALE REQUIREMENTS**

**NEW HPC DEPLOYMENTS**

**HPC USAGE MODELS** Including: Big data, HPC in clouds

**IMPROVE SYSTEM AND ENVIRONMENT CHARACTERISTICS** Including: Energy efficiency, System resilience

**BALANCE COMPUTE SUBSYSTEM, I/O AND STORAGE PERFORMANCE**
Transversal issues to be addressed

• Three technical topics:
  – Security in HPC infrastructures to support increasing deployment of HPDA
  – Resource virtualisation to increase flexibility and robustness
  – HPC in clouds to facilitate ease of access

• Two key element for HPC expansion
  – Usability at growing scale and complexity
  – Affordability (focus on TCO)
How was the SRA been built?

8 Workgroups covering the 8 technical focus areas:

**SRA 2015 technical focus areas**

- HPC System Architecture and Components
- Energy and Resiliency
- Programming Environment
- System Software and Management
- Big Data and HPC usage Models
- Balance Compute, I/O and Storage Performance
- Mathematics and algorithms for extreme scale HPC systems
- Extreme scale demonstrators

- 48 ETP4HPC member orgs/companies involved in these workgroups
- Members named 170 individual experts to contribute, 20-30 per working group
Other interactions

• Feedback sessions with end-users and ISVs at Teratec Forum
  – 20 end-users outline their deployment of HPC, future plans and technical recommendations
  – Very diverse set of priorities (performance & scale, robustness, ease of access, new workflows etc.)
  – No ‘One size fits all’ – approach possible

• Technical session with Big Data Value Association (BDVA) to understand architectural influences of HPDA
  – Technical dialogue started, much more to be done over next 1-2 years
  – BDVA will issue update to their SRIA in Jan 2016
The overall goals of the proposed research

- Exascale and extreme scale
- Ease-of-use
- Efficiency
  - energy
  - more globally TCO
- enabling both extreme data and extreme computing
- broadening of HPC use
The technical domains and the ESD proposal

Trends and recommended research topics – a few examples
HPC System Architecture, Storage and I/O, Energy and Resiliency

• Major trends - a subset:
  – Increased use of accelerators (e.g. GPUs, many core CPUs) in heterogeneous system architectures
  – Compute node architectures efficiently integrate accelerators, CPUs with high bandwidth memory
  – Non volatile memory types open up new interesting memory and caching hierarchy designs
  – System networks to significantly scale up and cut latencies, introducing virtualisation mechanisms
  – Storage subsystems to become more ‘intelligent’ to better balance compute and I/O
  – Increased activities in object storage technologies with major architectural revamp in the next years
  – Focus on architectural changes to improve energy efficiency and reduce data movement

• Research topics to be addressed (examples)
  – Compute node deep integration with embedded fast memory and memory coherent interfaces
  – Silicon photonics and photonic switching in HPC system networks
  – Global energy efficiency increases with targets of 60kW/PFlops in 2018 and 35 kW in 2020
  – Active storage technologies to enable ‘in situ’ and ‘on the fly’ data processing
  – Research in methods to manage ‘energy to solution’
  – Prediction of failures and fault prediction algorithms
## HPC System Architecture, Storage and I/O: milestones

| M-ARCH-1: New HPC processing units enable wide-range of HPC applications. | 2018 |
| M-ARCH-2: Faster memory integrated with HPC processors. | 2018 |
| M-ARCH-3: New compute nodes and storage architecture use NVRAM. | 2017 |
| M-ARCH-4: Faster network components with 2x signalling rate (rel. to 2015) and lower latency available. | 2018 |
| M-ARCH-5: HPC networks efficiency improved. | 2018 |
| M-ARCH-6: New programming languages support in place. | 2018 |
| M-ARCH-7: Exascale system energy efficiency goals (35kW/PFlops in 2020 or 20 kW/Pflops in 2023) reached. | 2020-2023 |
| M-ARCH-8: Virtualisation at all levels of HPC systems. | 2018 |
| M-ARCH-10: New components / disruptive architectures for HPC available. | 2019 |
| M-BIO-1: Tightly coupled Storage Class Memory I/O systems demo. | 2017 |
| M-BIO-2: Common I/O system simulation framework established. | 2017 |
| M-BIO-3: Multi-tiered heterogeneous storage system demo. | 2018 |
| M-BIO-4: Advanced IO API released: optimised for multi-tier IO and object storage. | 2018 |
| M-BIO-5: Big Data analytics tools developed for HPC use. | 2018 |
| M-BIO-6: ‘Active Storage’ capability demonstrated. | 2018 |
| M-BIO-7: I/O quality-of-Service capability. | 2019 |
| M-BIO-8: Extreme scale multi-tier data management tools available. | 2019 |
| M-BIO-9: Meta-Data + Quality of Service exascale file i/o demo. | 2020 |
| M-BIO-10: IO system resiliency proven for exascale capable systems. | 2021 |
### Energy and resiliency: milestones

<table>
<thead>
<tr>
<th>M-ENR-MS-1: Quantification of computational advance and energy spent on it.</th>
<th>2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>M-ENR-MS-2: Methods to steer the energy spent.</td>
<td>2017</td>
</tr>
<tr>
<td>M-ENR-MS-3: Use of idle time to increase efficiency.</td>
<td>2018</td>
</tr>
<tr>
<td>M-ENR-AR-4: New levels of memory hierarchy to increase resiliency of computation.</td>
<td>2017</td>
</tr>
<tr>
<td>M-ENR-FT-5: Collection and Analysis of statistics related to failures.</td>
<td>2018</td>
</tr>
<tr>
<td>M-ENR-FT-6: Prediction of failures and fault prediction algorithms.</td>
<td>2019</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>M-ENR-FT-10: Application survival on unreliable hardware.</th>
<th>2019</th>
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</thead>
<tbody>
<tr>
<td>M-ENR-AR-7: Quantification of savings from trade between energy and accuracy.</td>
<td>2018</td>
</tr>
<tr>
<td>M-ENR-AR-8: Power efficient numerical libraries.</td>
<td>2019</td>
</tr>
<tr>
<td>M-ENR-MS-9: Demonstration of a sizable HPC installation with explicit efficiency targets.</td>
<td>2019</td>
</tr>
</tbody>
</table>
System Software and Management, Programming Environment

• Major trends – a subset:
  – New node architectures demand innovative methods to solve scalability and concurrency issues
  – Network virtualisation and data security become critical system level challenges
  – Support for increasing use of ‘in situ’ data processing
  – Driven by HPDA, resource management needs to cope with highest levels of data allocation flexibility
  – Increased intelligence throughout the programming workflow
  – Productivity enhancements through use of domain specific languages (DSLs)
  – Interoperability and composability of programming models provide more flexibility to appl. developer

• Research topics to be addressed (examples)
  – Efficient OS support for heterogeneous architectures with complex memory hierarchies
  – Congestion control and adaptive/dynamic routing algorithms for exascale interconnects
  – Research on data-aware scheduling and resource management
  – Programming tool intelligence based on cost models for e.g. energy used, load-balancing, etc.
  – Programming models to allow for malleability (ability to adapt to changing resource availability)
# System Software and Management: milestones

<table>
<thead>
<tr>
<th>M-SYS-OS-1: Kernel scheduling policy.</th>
<th>2016</th>
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</thead>
<tbody>
<tr>
<td>M-SYS-OS-2: OS Low level standard API with run-time.</td>
<td>2017</td>
</tr>
<tr>
<td>M-SYS-OS-3: New memory management policy and libraries.</td>
<td>2017</td>
</tr>
<tr>
<td>M-SYS-OS-4: Container and virtualisation support; Hypervisor for HPC.</td>
<td>2016</td>
</tr>
<tr>
<td>M-SYS-OS-5: Offload programming model support.</td>
<td>2017-2019</td>
</tr>
<tr>
<td>M-SYS-OS-6: OS decomposition to add application performance and flexibility.</td>
<td>2019</td>
</tr>
<tr>
<td>M-SYS-OS-7: Investigate HPC specific security requirements on OS level.</td>
<td>2017-2019</td>
</tr>
<tr>
<td>M-SYS-IC-1: OS-bypass and hardware interface integrity protection.</td>
<td>2016</td>
</tr>
<tr>
<td>M-SYS-IC-2: Interconnect adaptive and dynamic routing algorithm and congestion control, power management.</td>
<td>2017</td>
</tr>
<tr>
<td>M-SYS-IC-3: Network virtualisation compliancy.</td>
<td>2017</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>M-SYS-CL-1: Flexible execution context configuration and management (from image to containers).</th>
<th>2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>M-SYS-CL-3: Infrastructure security.</td>
<td>2017-2020</td>
</tr>
<tr>
<td>M-SYS-RM-1: New Scalable scheduling enhancement, with execution environment and data provisioning integration.</td>
<td>2017</td>
</tr>
<tr>
<td>M-SYS-RM-3: Resilient framework.</td>
<td>2020</td>
</tr>
<tr>
<td>M-SYS-Vis-1: Scalable &quot;in situ&quot; visualisation.</td>
<td>2016</td>
</tr>
<tr>
<td>M-SYS-Vis-2: Scaling for the compositing phase.</td>
<td>2017</td>
</tr>
<tr>
<td>M-SYS-Vis-3: Ray-tracing capabilities.</td>
<td>2018</td>
</tr>
<tr>
<td>M-SYS-Vis-4: High dimensional data, graphs and other complex data topologies.</td>
<td>2018</td>
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</tbody>
</table>
## Programming Environment: milestones

<table>
<thead>
<tr>
<th>Milestone Code</th>
<th>Description</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>M-PROG-API-1</td>
<td>Develop benchmarks and mini-apps for new programming models/languages.</td>
<td>2016</td>
</tr>
<tr>
<td>M-PROG-API-2</td>
<td>APIs and annotations for legacy codes.</td>
<td>2017</td>
</tr>
<tr>
<td>M-PROG-API-3</td>
<td>Advancement of MPI+X approaches (beyond current realisations).</td>
<td>2017</td>
</tr>
<tr>
<td>M-PROG-API-4</td>
<td>APIs for auto-tuning performance or energy.</td>
<td>2017</td>
</tr>
<tr>
<td>M-PROG-API-5</td>
<td>Domain-specific languages (specific languages and development frameworks).</td>
<td>2018</td>
</tr>
<tr>
<td>M-PROG-API-6</td>
<td>Efficient and standard implementation of PGAS.</td>
<td>2018</td>
</tr>
<tr>
<td>M-PROG-API-7</td>
<td>Non-conventional parallel programming approaches (i.e. not MPI, not OpenMP / pthread / PGAS - but targeting asynchronous models, data flow, functional programming, model based).</td>
<td>2019</td>
</tr>
<tr>
<td>M-PROG-LIB-1</td>
<td>Self- / auto-tuning libraries and components.</td>
<td>2018</td>
</tr>
<tr>
<td>M-PROG-LIB-2</td>
<td>Components / library interoperability APIs.</td>
<td>2017</td>
</tr>
<tr>
<td>M-PROG-LIB-3</td>
<td>Templates / skeleton / component based approaches and languages.</td>
<td>2019</td>
</tr>
<tr>
<td>M-PROG-RT-1</td>
<td>Run-time and compiler support for auto-tuning and self-adapting systems.</td>
<td>2018</td>
</tr>
<tr>
<td>M-PROG-RT-2</td>
<td>Management and monitoring of run-time systems in dynamic environments.</td>
<td>2018</td>
</tr>
<tr>
<td>M-PROG-RT-3</td>
<td>Run-time support for communication optimisation and data placement: data locality management, caching, and prefetching.</td>
<td>2019</td>
</tr>
<tr>
<td>M-PROG-RT-4</td>
<td>Enhanced interaction between run-time and OS or VM monitor (w.r.t. current practice).</td>
<td>2018</td>
</tr>
<tr>
<td>M-PROG-RT-5</td>
<td>Scalable scheduling of million-way multi-threading.</td>
<td>2020</td>
</tr>
<tr>
<td>M-PROG-DC-1</td>
<td>Data race condition detection tools with user-support for problem resolution.</td>
<td>2017</td>
</tr>
<tr>
<td>M-PROG-DC-2</td>
<td>Debugger tool performance and overheads (in CPU and memory) optimised to allow scaling of code debugging at peta- and exascale</td>
<td>2018</td>
</tr>
<tr>
<td>M-PROG-DC-3</td>
<td>Techniques for automated support for debugging (static, dynamic, hybrid) and anomaly detection, and also, for the checking of programming model assumptions.</td>
<td>2018</td>
</tr>
<tr>
<td>M-PROG-DC-4</td>
<td>Co-design of debugging and programming APIs to allow debugging to be presented in the application developers original code, and also, to support applications developed through high-level model descriptions.</td>
<td>2018</td>
</tr>
<tr>
<td>M-PROG-PT-1</td>
<td>Scalable trace collection and storage: sampling and folding.</td>
<td>2018</td>
</tr>
<tr>
<td>M-PROG-PT-2</td>
<td>Performance tools using programming model abstractions.</td>
<td>2018</td>
</tr>
<tr>
<td>M-PROG-PT-4</td>
<td>Performance analytics tools.</td>
<td>2018</td>
</tr>
<tr>
<td>M-PROG-PT-5</td>
<td>Performance analytics at extreme scale.</td>
<td>2019</td>
</tr>
</tbody>
</table>
Big Data and HPC Usage Models, Mathematics and Algorithms

• Major trends – a subset:
  – Data analytics, including visualisation increasingly will take place ‘in situ’
  – HPC systems with lots of memory and fast networks become ideal compute infrastructure for Big Data
  – Focus on math and algorithms for exascale system software (compilers, libraries, programming environment)
  – Advances in mathematical methods req. to improve energy efficiency by two orders of magnitude

• Research topics to be addressed (examples)
  – Research on new performance metrics to reflect data-centric use of HPC infrastructure
  – Data centric memory hierarchies and architectures, data structure transformation to enable HPDA
  – Systematic analysis of data flows in key Big Data applications to minimise data access and movement
  – Research on HPC and Big Data hybrids to allow simulation and data analytics at the same time
  – Mathematical support for data placement and data movement minimization
  – Research on the impact of algorithmic and mathematical advances to programming tools
  – Work on new algorithms to reduce energy to solution
### Big Data and HPC Usage Models, mathematics and algorithms

<table>
<thead>
<tr>
<th>Project Code</th>
<th>Description</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>M-BDUM-METRICS-1</td>
<td>Data movement aware performance metrics.</td>
<td>2017</td>
</tr>
<tr>
<td>M-BDUM-METRICS-2</td>
<td>HPC like performance metrics for Big Data systems.</td>
<td>2017</td>
</tr>
<tr>
<td>M-BDUM-METRICS-3</td>
<td>HPC-Big Data combined performance metrics.</td>
<td>2018</td>
</tr>
<tr>
<td>M-BDUM-MEM-1</td>
<td>Holistic HPC-Big Data memory models.</td>
<td>2017</td>
</tr>
<tr>
<td>M-BDUM-MEM-2</td>
<td>NVM-HPC memory and Big Data coherence protocols and APIs.</td>
<td>2017</td>
</tr>
<tr>
<td>M-BDUM-ALGS-1</td>
<td>Berkeley Dwarfs determination for Big Data applications.</td>
<td>2017</td>
</tr>
<tr>
<td>M-BDUM-ALGS-2</td>
<td>Implementations of Dwarfs in Big Data platforms.</td>
<td>2019</td>
</tr>
<tr>
<td>M-BDUM-PROG-1</td>
<td>Hybrid programming paradigms HPC-Big Data.</td>
<td>2017</td>
</tr>
<tr>
<td>M-BDUM-PROG-2</td>
<td>Hybrid programming paradigm with coherent memory and compute unified with Big Data programming environments.</td>
<td>2018</td>
</tr>
<tr>
<td>M-BDUM-PROG-3</td>
<td>Single programming paradigm across a hybrid HPC-Big Data system.</td>
<td>2021</td>
</tr>
<tr>
<td>M-BDUM-VIRT-1</td>
<td>Elastic HPC deployment.</td>
<td>2018</td>
</tr>
<tr>
<td>M-BDUM-VIRT-2</td>
<td>Full virtualisation of HPC usage.</td>
<td>2021</td>
</tr>
<tr>
<td>M-BDUM-DIFFUSIVE-1</td>
<td>Big Data - HPC hybrid prototype.</td>
<td>2017</td>
</tr>
<tr>
<td>M-BDUM-DIFFUSIVE-2</td>
<td>Big Data - HPC large-scale demonstrator.</td>
<td>2020</td>
</tr>
</tbody>
</table>
Mathematics and algorithms for extreme scale HPC systems: milestones

<table>
<thead>
<tr>
<th>M-ALG-1</th>
<th>Scalability of algorithms demonstrated for forward in time computing for current architectures. 2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>M-ALG-2</td>
<td>Multiple relevant use cases demonstrated for improving performance by means of robust, inexact algorithms. 2018</td>
</tr>
<tr>
<td>M-ALG-3</td>
<td>Scalable algorithms demonstrated for graph-based analytics. 2019</td>
</tr>
<tr>
<td>M-ALG-4</td>
<td>Processes established for co-design of mathematical methods for data analytics and of HPC technologies/architectures. 2019</td>
</tr>
<tr>
<td>M-ALG-5</td>
<td>Classes of data, partitioning and scheduling problems categorised and their complexity ascertained. 2019</td>
</tr>
<tr>
<td>M-ALG-6</td>
<td>Mathematical and algorithmic approaches established for the scheduling of tasks on abstract resources and exploitation of multiple memory levels. 2020</td>
</tr>
<tr>
<td>M-ALG-7</td>
<td>Research on mathematical methods and algorithms exploited for compiler technologies, run-time environments and related tools. 2018</td>
</tr>
<tr>
<td>M-ALG-8</td>
<td>Reduction of energy-to-solution demonstrated by means of appropriately optimized algorithms demonstrated for a set of relevant use cases. 2017</td>
</tr>
<tr>
<td>M-ALG-9</td>
<td>Process for vertical integration of algorithms established together with the validation of scalability, ease of implementation, tuning and optimisation. 2019</td>
</tr>
</tbody>
</table>
Extreme-Scale Demonstrators

• Characteristics
  – Complete prototype HPC systems
  – high enough TRL to support stable production
  – using technologies developed in the previous projects
  – based on application – system co-design approach
  – large enough to address scalability issues (at least 1/10 of top performance systems)

• Two project phases:
  – phase A : development, integration (of results from R&D projects) and testing
  – phase B : deployment and use, code optimisation, assessment of the new technologies
Extreme scale Demonstrators call-integration-deployment schedule

WP 2014/15 (project execution)

WP 2016 (project execution)

3Q 2015

4Q 2016

4Q 2016

EsD 1-2 projects

EsD 3-4 projects

EsD call

EsD integration

EsD deployment

4Q 2017

2Q 2018

1Q 2020

2Q 2022

4Q 2018

2Q 2019

1Q 2021

2Q 2023

EsD 1

EsD 2

EsD 3

EsD 4

P1

P2

... Pn

P1

P2

... Pm

3Q 2015

4Q 2016

4Q 2017

2Q 2018

1Q 2020

2Q 2022

4Q 2018

2Q 2019

1Q 2021

2Q 2023

WP 2014/15

WP 2016

EsD call

EsD integration

EsD deployment
SRA 2015 – Status
SRA 2015

• Posted on ETP4HPC website 24th Nov 2015 and disseminated via different media

• Public **Call for Comments** on SRA 2 - opened 9th Dec 2015 ([http://www.etp4hpc.eu/strategic-research-agenda/](http://www.etp4hpc.eu/strategic-research-agenda/)) and also LinkedIn, Twitter and EXDCI project

• **Next actions**
  
  • 1Q 2016
    
    ➢ Facilitate interactions with WP14/15 projects
    
    ➢ Interactions with EXDCI WP3 (application development)
    
    ➢ next technical workshop with BDVA experts to prepare next SRA 3 updates

  • 3Q 2016
    
    ➢ based on feedback received and interactions (workshops): define areas needing updates
    
    ➢ prepare for next update cycle, target date 31st July 2017
Google

« Public Call for comments on SRA »
Next SRA-related events – some thoughts

• HPC summit/May 2016
  – needs to be focused primarily on the EsD topic (we need to make some progress here), not so much on the dissemination
  – at this event the three pillars for the EsD mission (CoE, HPC centres and the FETHPC1 project speakers) need to get together...

• ISC16
  – might be a general dissemination and discussion event
  – by then we have some feedback hopefully
  – depending on how much progress we make with BDVA we could set up a few "focused discussions", e.g. on HPC and HPDA, EsDs, some statistics on the feedback received, news on influences from latest application trends....etc.
Conclusion
Collaboration opportunity

• Some of the challenges are similar

• We will welcome your comments on the current SRA

http://www.etp4hpc.eu/strategic-research-agenda/

• You can participate in HPC events: HPC Summit, ISC2016

• You are welcome to participate in the expert group for the next version (targeted in 1H2017)
THANK YOU!

For more information visit 

www.etp4hpc.eu

contact: office@etp4hpc.eu