Mont-Blanc 3, European scalable and power efficient HPC platform based on low-power technology

MB3 project highlights (5 -8 lines)

The main target is the creation of a new high-end HPC platform (SoC and node) that is able to deliver a new level of performance / energy ratio whilst executing real applications.

The technical objectives are:

1. To design a well-balanced architecture and to deliver the design for an ARM based SoC capable of providing pre-exascale performance (measured using real HPC applications) when implemented in the time frame of 2019-2020.

2. To maximize the benefit for HPC applications with new high-performance ARM processors and throughput-oriented compute accelerators designed to work together within the well-balanced architecture.

3. To develop the necessary software ecosystem for the future SoC.

•What are anticipated technology (hw/sw/methodology) suggested for inclusion in an EsD project and describe the current maturity?

• MB3 software ecosystem (aligned with OpenHPC) – high maturity level

• MB3 chip design, permitting to initiate the development of an HPC SoC

• MB3 multiscale simulation infrastructure – key for design & performance extrapolations

• MB3 test-platform platform (based on Sequana architecture) – announced in January

•How should this technology be used / integrated (I/F, APIs)

•Are there any pre-or co-requisite items

- The compute SoCs needs to be provided/developed

•Any extra work/interaction (on top of current project roadmap) needed to make them ready?

- The software environment – although being currently relatively extensive – shall need further developments

•What information / actions are needed to best prepare for EsD projects?

- Extensive information about complementary technological bricks
- Consolidated EsD roadmap information