ExaNoDe investigates, develops, integrates and validates the building blocks for a highly efficient, highly integrated, high-performance, heterogeneous compute element aimed towards Exascale computing. It addresses those targets through the coordinated application of several innovative solutions recently deployed in HPC: ARM-v8 low-power processors for a good balance between energy efficiency and computational power, 3D integration for compute density with interposer-based nodes built from several chips (so called chiplets) stacked on a silicon interposer, and a novel Global Address Space memory system (UNIMEM) for low-latency and high-bandwidth memory access, with the potential to scale to Exabyte levels. The project will deliver a prototype that will enable the deployment of interposer-based compute nodes and the evaluation, tuning and analysis of HPC critical kernels along with the associated software stack.

ExaNoDe is a technology development project steered by HPC application knowledge and kernels. The following technology results are suggested for inclusion in an EsD project:

Technology	Type	Description
Compute Element	ExaNoDe prototype	Integrated device (HW and SW) mounted on a PCB with physical and logical characteristics that make it compatible for use into both commercially available blades, and on the mezzanine carrier boards being developed in the ExaNeSt project.
Integration	Methodology	Skills and knowledge associated with the integration into a single package of several silicon bare dies (unpackaged components).
Low-Power Processor	FPGA firmware	FPGA logic in terms of hardware IP and enabling software which links the CPU (ARM Cortex-A53) and the FPGA fabric to create the many-core scalability model for this device based on UNIMEM.
Accelerator	FPGA firmware	FPGA reconfigurable fabric in which custom accelerators can be inserted into the system's memory hierarchy.
	HW IP for SoC	Hardware accelerated convolutional neural network (CNN) for deep learning.
Network on chip (NoC)	HW IP	Extended NoC technology for linking different stacked silicon dies on an active silicon interposer.
Enhanced 2.5D interface	HW IP	Chip-to-chip interface for fast and low-power inter-chip communication via the interposer.
Unimem IPs	HW IPs	Two HW IPs (the Virtualized Packetizer and the Virtualized Mailbox) to support remote atomic operations.
Checkpointing of VMs	SW extension	Technology for live-memory snapshots based on a post-copy and incremental checkpoint (with KVM).
Virtualization with Unimem	SW IP (API and libraries)	Technology to virtualize the services made available by UNIMEM.
Programming models	SW IP	GPI-2, MPI, OmpSs and OpenStream extended to use UNIMEM.
Thermal and Power Management	SW IP	Software component which uses internal power and thermal prediction to select the operating frequency of the cores in a multicore device.

In terms of maturity, all of the above technologies will be integrated and validated into the ExaNoDe prototype. They are designed to be as generic as possible, but extra work for adaptation into specific project requirements may be required. Hardware will predominantly be made available using commercial licences while software will be predominantly made available using open-source licences. Detailed information is available in the public deliverable "D6.4 Technology Transfer Strategy Document" shortly downloadable from the ExaNoDe website: http://exanode.eu/.